ONFi 2.1 – Delivering Increased Performance and Functionality for NAND Flash Components

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NAND Standardization Needed

- NAND has been the only commodity memory with no standard interface
  - Command set, timings, and pin-out are similar among vendors
- NAND has been ripe for standardization due to a few inflection points:
  - 1) Explosion in use of NAND for MP3s, phones, caches, and SSDs
  - 2) Increase in NAND suppliers serving the market (2 to ~7)
- ONFi Workgroup was formed in May 2006 to address need
  - ONFi = Open NAND Flash Interface
- ONFi revision 1.0 delivered in December 2006, defines:
  - Uniform NAND electrical and protocol interface
    - Raw NAND component interface for embedded use
    - Includes timings, electrical, protocol
    - Standardized base command set
  - Uniform mechanism for device to report its capabilities to the host

ONFi 1.0 sets a solid foundation for NAND standardization.

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ONFi enjoys the support of over 80 members.

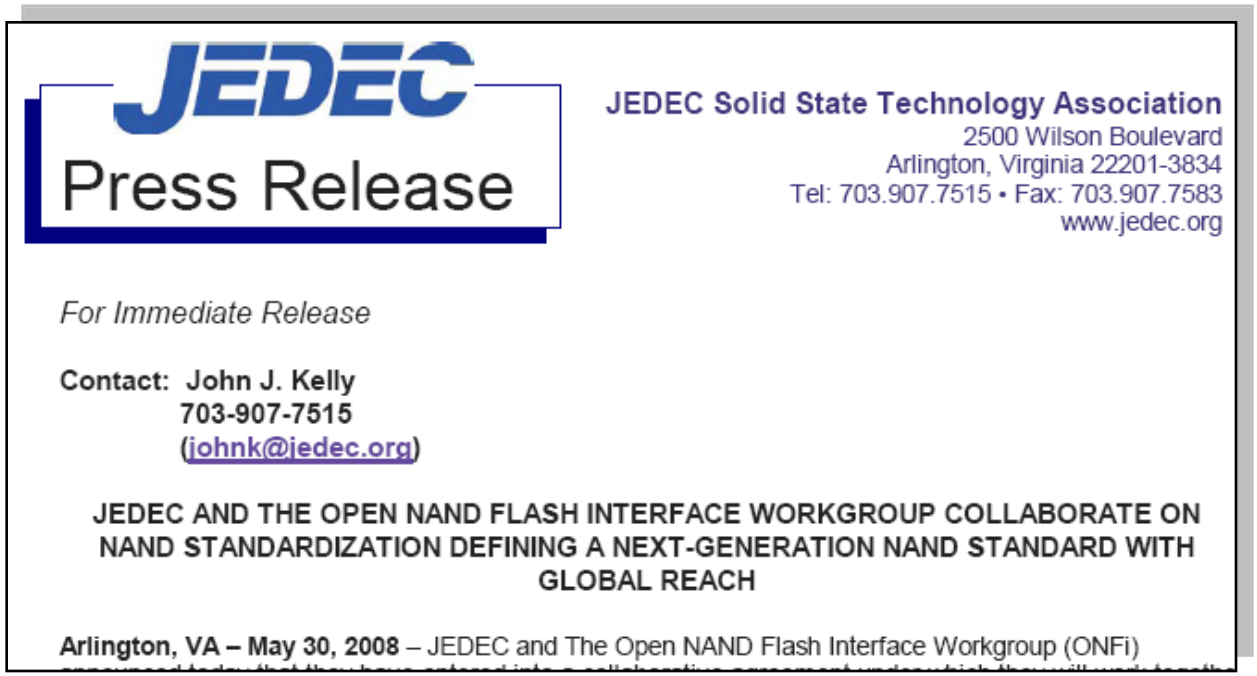
Conveying the Benefits of ONFi

- A revamped ONFi website conveys to end users and customers the benefits that ONFi brings and provides easy access to ONFi technical information

Regularly check the ONFi website at www.onfi.org to stay informed on the latest changes in the ONFi world.

JEDEC and ONFi Collaborating

- The ONFi Workgroup is pleased to team up with JEDEC on NAND standardization moving forward
- ONFi has submitted the ONFi 2.0 specification as part of the joint effort



JEDEC

Press Release

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JEDEC AND THE OPEN NAND FLASH INTERFACE WORKGROUP COLLABORATE ON NAND STANDARDIZATION DEFINING A NEXT-GENERATION NAND STANDARD WITH GLOBAL REACH

Arlington, VA – May 30, 2008 – JEDEC and The Open NAND Flash Interface Workgroup (ONFi)

Any ONFi or JEDEC member may participate in the ONFi-JEDEC Joint Taskgroup.

Rapidly Delivering Innovation

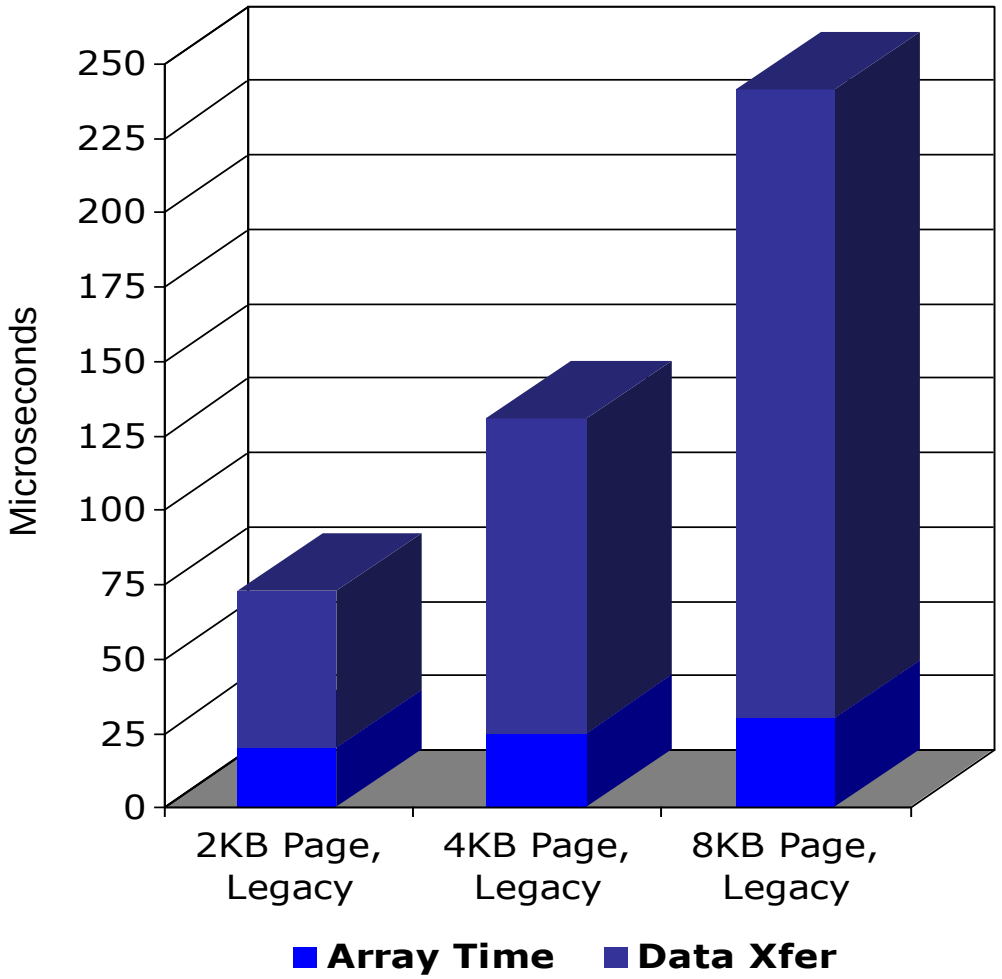
- The ONFi Workgroup has been very productive, delivering three specifications over the course of 2007 / early 2008
  - Block Abstracted NAND in July ’07
  - ONFi 2.0, including high speed DDR interface, in February ’08
  - NAND Connector definition in April ‘08

ONFi OPEN NAND FLASH INTERFACE

The Latest Innovation: ONFi 2.1

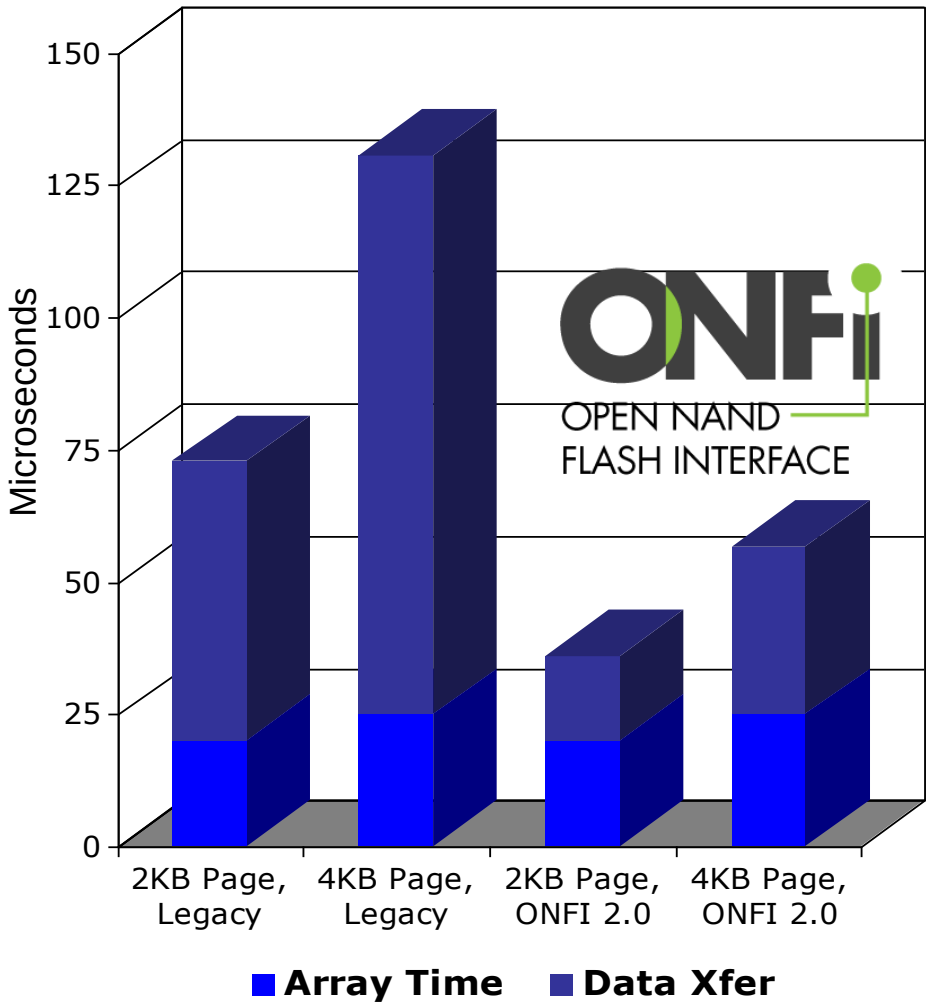
- ONFi 2.1 was ratified in mid-January and contains a plethora of new features
- New features include:
  - 166 MB/s and 200 MB/s speeds
  - Power management enhancements
  - Enhanced ECC information
  - New commands for increased performance and functionality
- The remainder of this webcast will provide an overview of the features ONFi 2.1 brings

Limited Performance with Legacy NAND Bus



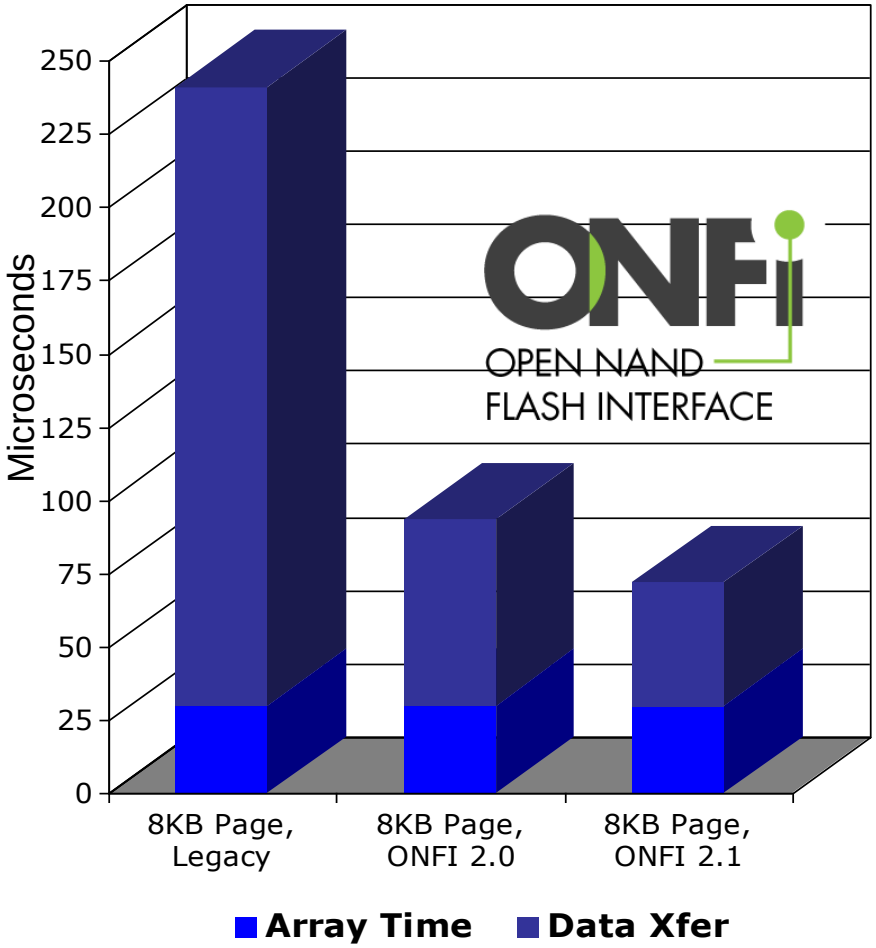
- NAND component performance is determined by two elements
  - NAND array access time
  - Data transfer across the bus
- For legacy reads, performance is artificially limited to 40 MB/s
- As NAND page sizes increase, latency for transferring a page becomes very large
  - Especially for small reads

ONFi 2.0 Unleashed
NAND Performance



- ONFi 2.0 defined the source synchronous DDR interface with speeds up to 133 MB/s
  - More than 3x improvement!
- For 2KB and 4KB NAND page sizes, this brought array and data transfer time in balance
- With pipelined reads, the array time can be hidden allowing for sustained 133 MB/s transfers

ONFi 2.1 Extends Gains, Especially as Page Size Increases



- ONFi 2.1 defines 166 MB/s and 200 MB/s speed grades
- With 8KB NAND page sizes on advanced lithographies, data transfer time is again double the array time
- The 200 MB/s speed grade brings back balance between the array and data transfer times
  - It also further decreases latency for receiving first page from NAND array in a read burst

200 MB/s speed ensures NAND performance remains array limited, getting maximum benefit from the NAND.

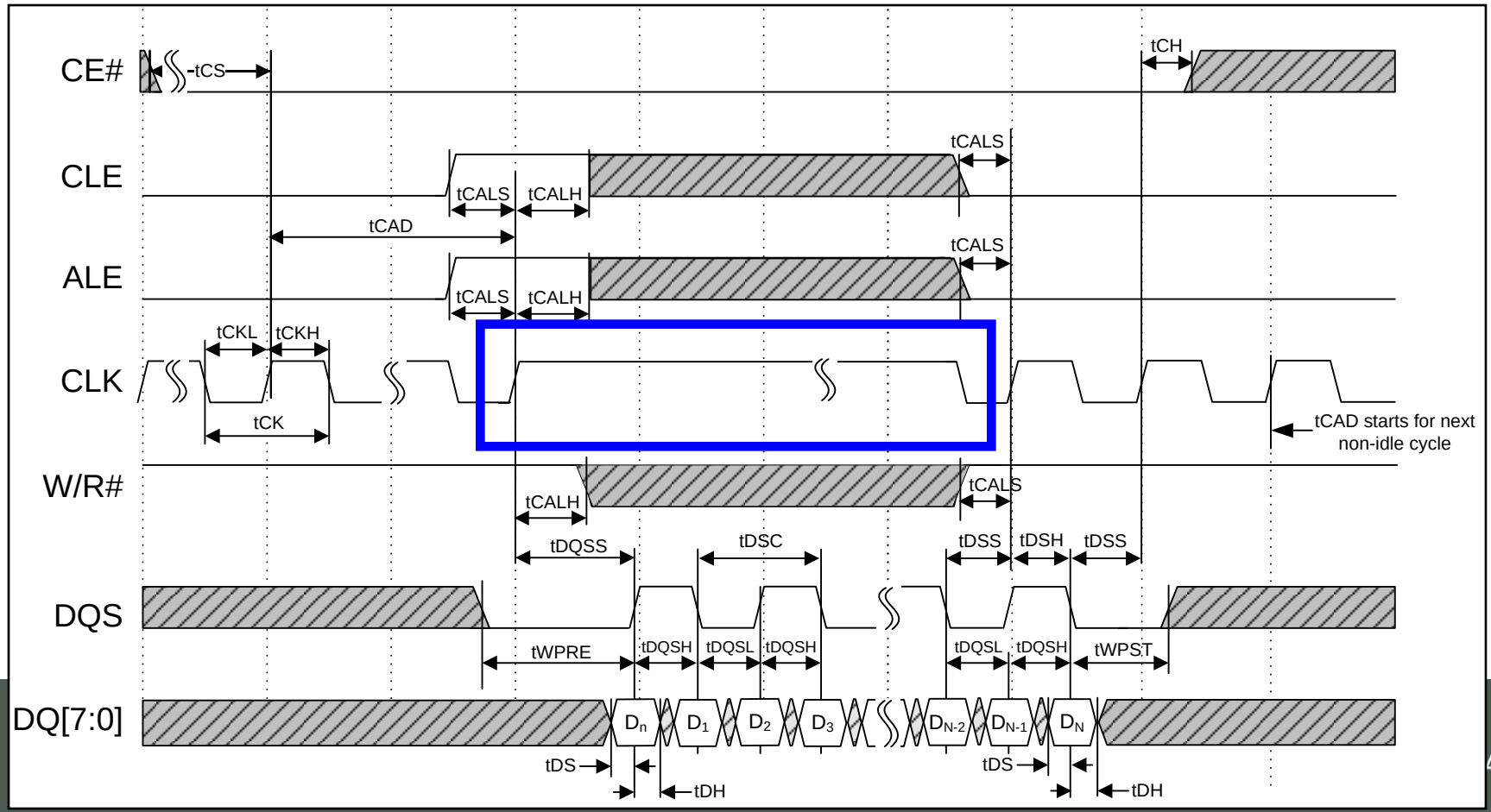
ONFi: The Speed You Need

- ONFi defines speeds ranging from 40 MB/s to 200 MB/s, to allow applications to balance performance and power
- The new speeds defined in ONFi 2.1 are 166 MB/s (mode 4) and 200 MB/s (mode 5)

Parameter	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
	50		30		20		15		12		10		ns
	~20		~33		~50		~66		~83		~100		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tAC	—	20	—	20	—	20	—	20	—	20	—	20	ns
tADL	100	—	100	—	70	—	70	—	70	—	70	—	ns
tCADf	25	—	25	—	25	—	25	—	25	—	25	—	ns
tCADs	45	—	45	—	45	—	45	—	45	—	45	—	ns
tCAH	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCALH	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCALS	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCAS	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCH	10	—	5	—	4	—	3	—	2.5	—	2	—	ns
tCK(avg) or tCK	50	—	30	—	20	—	15	—	12	—	10	—	ns
...													

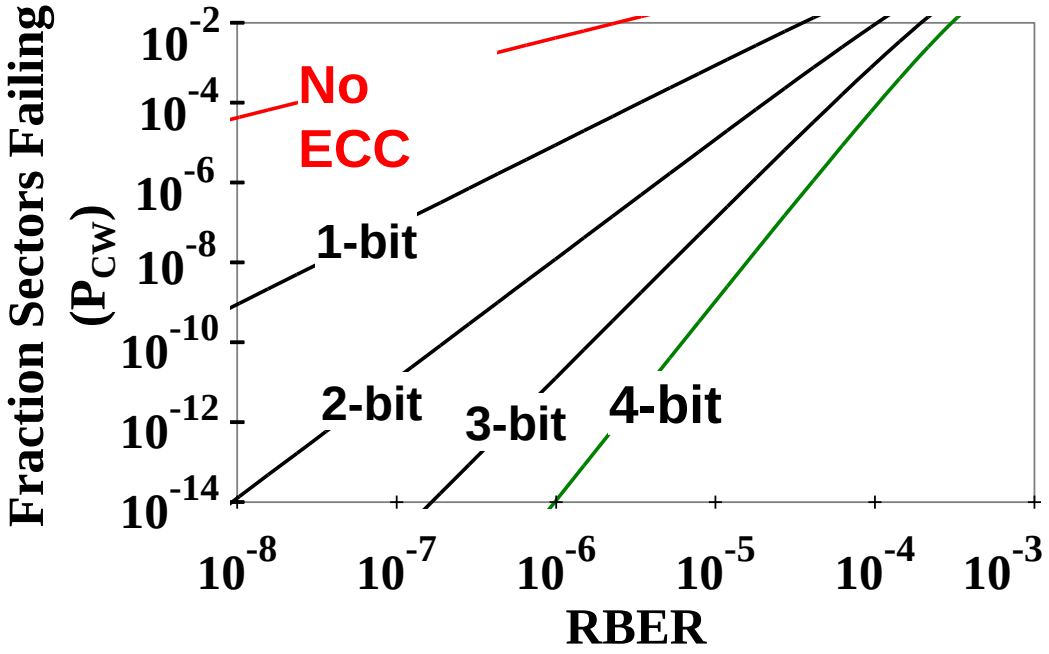
Saving Power Wherever Possible

- To decrease power during writes to the NAND, ONFi 2.1 allows the host to stop the clock during writes
  - Savings of 10s of milliwatts are possible with this technique



ECC Requirements Growing

- ECC is required to correct for bit errors that naturally occur with NAND
- As the raw bit error (RBER) of NAND increases, the amount of ECC applied goes up
- Communicating error correction needs effectively is critical



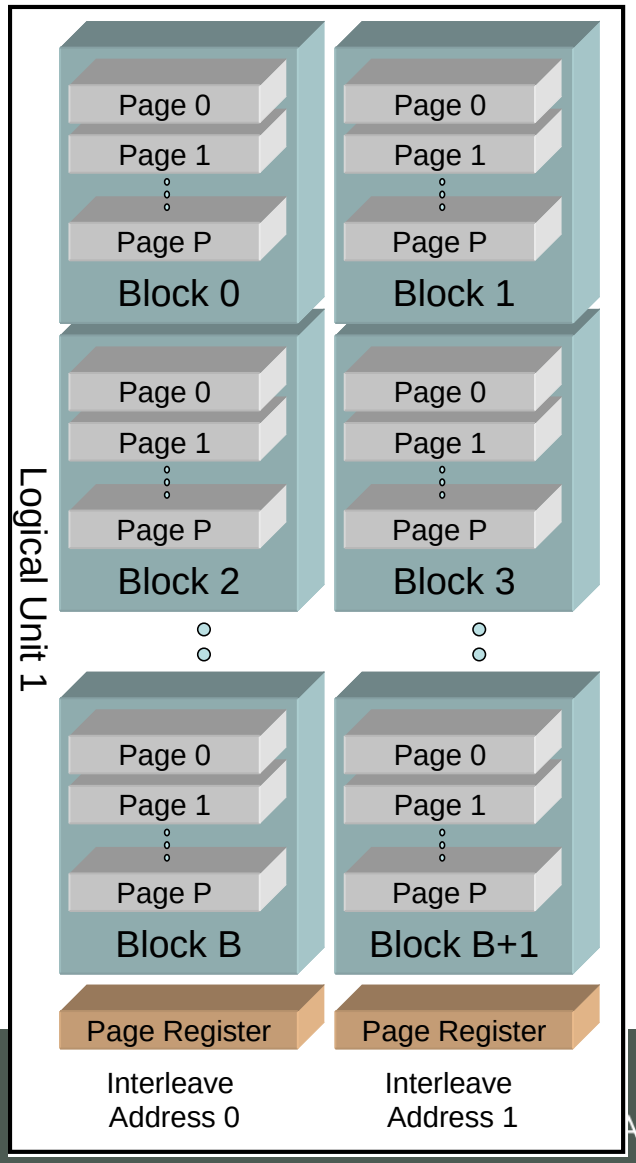
Communicating ECC Effectively

- For ECC, a set of parameters have to be looked at holistically as they are intimately related; the parameters are:
  - ECC codeword size
  - Number of bits to correct anywhere within the codeword
  - Number of program/erase cycles (distributed)
  - Number of valid blocks
- ONFi 2.1 allows the NAND device to communicate these parameters together in the *Extended ECC Information*
- The device may communicate multiple sets of these parameters, if the NAND may be used in different environments (e.g. server, client, netbook)
  - The NAND device could indicate parameters for three different block endurance values (e.g. 1,000, 10,000 and 100,000 cycles)
  - The device can communicate the needed codeword size, which likely will grow from 512B to 1KB to avoid large increases in spare area

Byte	Definition
0	Number of bits ECC correctability
1	Codeword size
2-3	Bad blocks maximum per LUN
4-5	Block endurance
6-7	Reserved

Interleaved Reads for More Performance

- A logical unit (LUN) may support interleaved addressing
- This allows two or more of the same type of operation to execute concurrently
- ONFi 2.1 has added support for interleaved reads
- Enables deeper pipelining of reads, especially in MLC situations where the array time may be longer

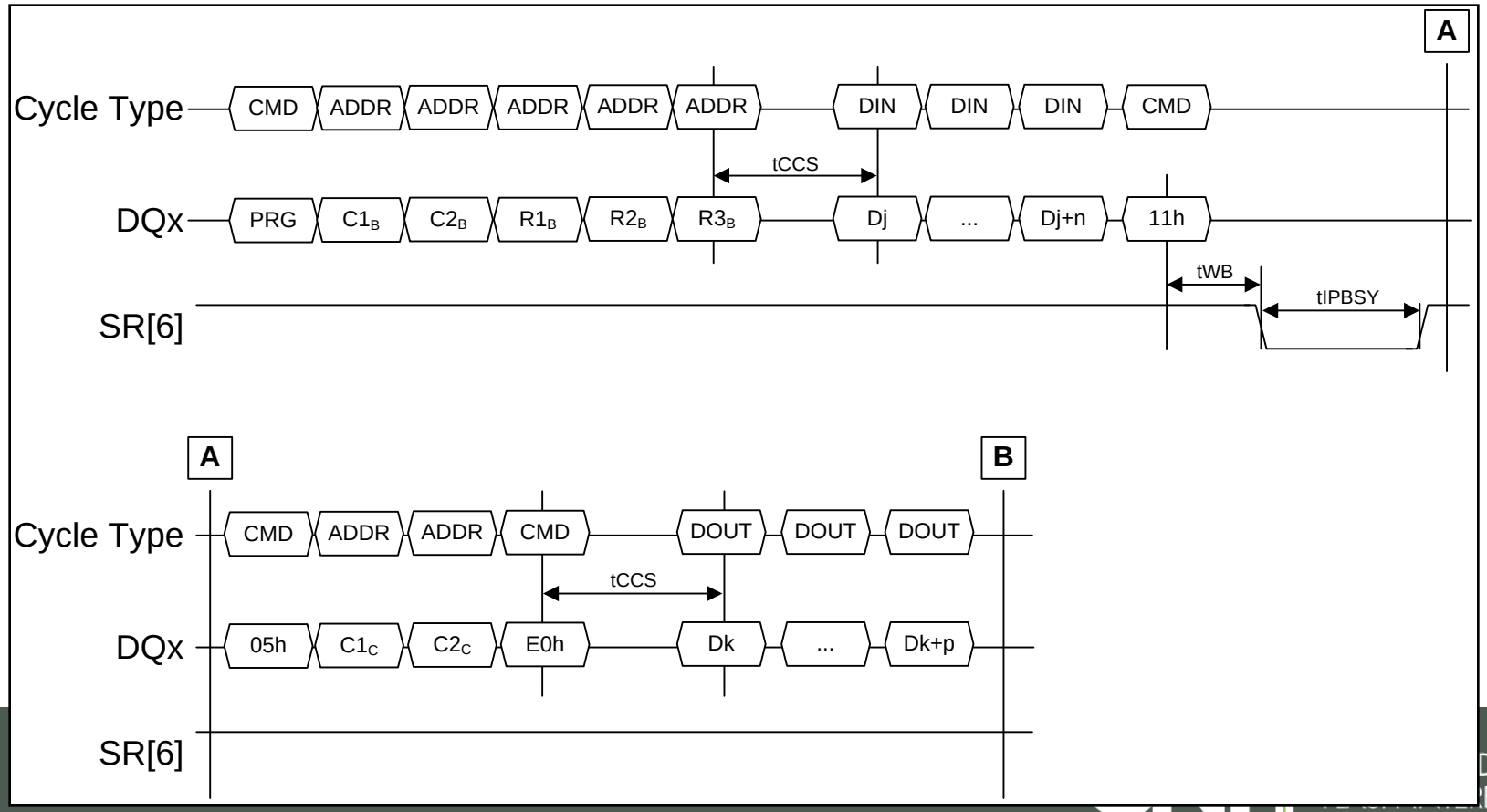


Enabling Low Cost Controllers

- For Copyback operations, low cost controllers are forced to have internal SRAM that is a minimum of the NAND page size
- This requirement is necessary to allow the controller to correct ECC errors from the pages read as part of the Copyback
- ONFi 2.1 has eliminated this storage requirement by introduction of the Small Data Move command

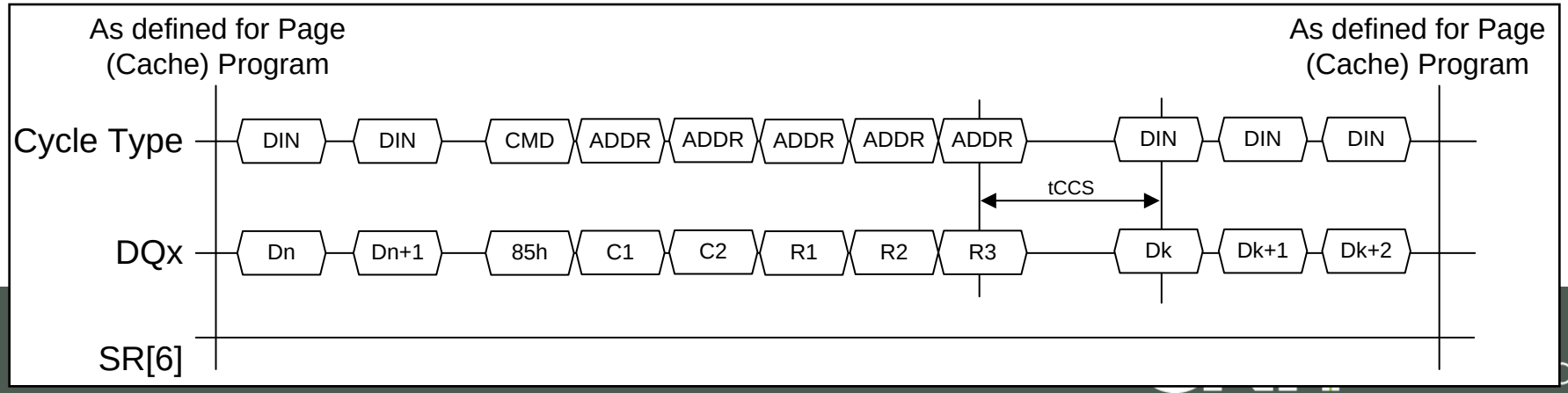
Small Data Move Detail

- Small Data Move allows a portion of data to be written, followed by more data output



Making NAND Better for Card Applications

- In MMC and SD applications, there are commands that allow the host to write indefinitely
  - When the host stops writing, it may be in the middle of a page which is awkward for the NAND
- ONFi 2.1 introduces the Change Row Address command.
  - Change Row Address changes the location the page is being written to, avoiding writing an incomplete page to the final location
  - Firmware can then perform read/modify/write actions and write the complete page to the originally targeted location



Summary

- ONFi is delivering innovation to move NAND forward
  - ONFi 1.0, Block Abstracted NAND, ONFi 2.0, NAND Connector, and ONFi 2.1 all delivered over the course of ~ 3 years
- ONFi 2.1 delivers enhancements for the gamut of applications NAND is used in
  - Speed grades up to 200 MB/s for applications like SSDs
  - New commands that help low cost implementations and cards
- ONFi is continuing its mission to bring value to NAND, including a productive collaboration with JEDEC

Get involved with ONFi.
Visit www.onfi.org for more information.

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