Open NAND Flash Interface Specification

Revision 6.0
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Micron Technology, Inc.
Phison Electronics Corp.
Western Digital Corporation
SK Hynix, Inc.
Sony Corporation

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ONFI Workgroup Technical Editor:

mailto: ONFI Admin
Email: onfiadmin@onfi.org

Revision History

Revision Number	Description	Author	Revision Date
Draft 0.0	• Initial draft	Rey de Luna	Aug 20, 2024
Draft 0.1	• Removed solder ball diameter sizes for 132b and 152b packages in section 2.1 BGA-152 and BGA-132 Ball Assignments • Modified statement in Section 2.3 BGA-178, BGA-154, and BGA-146 Ball Assignments to add 10x14mm as possible size for 146b package. • Modified signal mapping tables Table 2-4, Table2-5, Table 2-6 to remove optional description of some VCCQ and VCCQL balls and consolidated balls to mandatory “VCCQ or VCCQL” row. Separated out signals which were optional for VCCQ or VCCQL. • Added IST spec clarifications to Table 2-10 and section 2.10.1 that it applies to Vcc supply • Modified Table 4-1 NV-LPDDR4 with VccQL (PI-LTT) maximum data rate from Vendor Specific (VSP) to 4800MT/s with note that maximum achievable on a vendor device is vendor specific • Updated Fig. 4-1, Fig. 4-3, Fig. 4-22, Fig. 4-23, Fig. 5-13, Fig. 5-14 to reflect unmatched DQS timings • Corrected typos in section 4.5 and updated Fig. 4-5 to show optional initial DQS oscillator step • Edited 4.13 On-Die Termination (ODT) section to improve sentence organization and applicability and added references to pertinent SCA sections. • Overhauled 4.16.1.5 and updated section title to “Conv. and SCA Protocol Data Input Skew Specs” • Fixed error in Fig. 6-34. • Corrected Table 4-36 TM26 tDIVW1 value and re-titled table to more descriptive label • Updated Table 4-37 TM23 thru TM26 tDVWp values from 0.6UI to 0.57UI • Updates to several bytes in 6.7.1 Parameter Page Data Structure Definition: bytes 4-5, 15, 100, 105-106, 107, 108-109, 110, 118-121, 164-165 • Corrected Table 8-1 FA42h to Reserved	Rey de Luna	Jan 07, 2025
Draft 0.2	• Under section 2.2, updated 316b package ballmaps (Figures 26 and 27): added “_n” to R/B signal names and swapped SCA_0 and SCA_1 locations • Under section 2.4, Table 25, swapped SCA_0 and SCA_1 locations • Under section 2.13, retitled section to “Power Sequence and Ready/Busy (R/B_n) Requirements”. Retitled "Power-On Requirements" sub-section to "Power Sequence Requirements". Under “Power Sequence Requirements” sub-section, added VccQL to Figure 2-19 and retitled table to "Power-On Sequence and R/B_n Power-On Behavior", added VccQ versus VccQL requirements and figure.	Rey de Luna	Sep 08, 2025

	• Under section 4.7 Test Conditions, updated Input Slew Rate specifications in Table 4-5 Test Conditions for Timing Specs. • Under 4.12 Warmup Cycle section, added new 4.12.1 Progressive Warmup Cycles sub-section. • Under section 4.14.1 General Timing Parameters, under Table 4-28 General Interface Timing Parameters table, edited Note 3 for Conv. Protocol from “tWB starts on the last rising edge of DQS" to "tWB starts on the last falling edge of DQS", under Table 4-32 ZQ Calibration Timing parameters, relaxed tZQCL from 1.0uS to 1.2uS • Under section 4.14.2 Data Burst Related Parameters, under Table 4-33, changed tDQSD SCA applicability to “No”. • Under 5.9 DQ Bus Control Packets section, updated figures for SCE, SCP, SCT to show last bit as VSP • Under 5.9.2 Select Chip Pause (SCP) Packet section, added restriction that SCP packet is required prior to resuming paused data burst • Under 5.9.5 Data Output Burst Sequence, removed tDQSD from figures 5-16 and 5-17. • Under 5.10 LUN Selection (LUNSel) Packet (Optional) section, updated figures 5-23 and 5-24 to show last bit in LUNSel packet as VSP • Under section 5.12.2 Program Sequence, modified Figure 5-29 by adding a more detailed diagram depicting tCDL. • Under section 5.17.1 SCA Protocol AC and DC Operating Conditions, under SCA Protocol CA Pins Output Accuracy table, changed R_SCA_CApupd_mismatch Minimum to -25.0 ohms. • Retitled Appendix D to 12. Appendix: ICC/ICCQ Measurement Methodology. Split appendix, one sub-section for Conv. Protocol and added new section for SCA Protocol.		
Draft 0.3	• Updated section 3.3 Factory Defect Mapping to incorporate new FBB Scan via Read Status method. • Under section 4.15, relaxed tAC min and tDQSRE min specs to 1ns in Table 4-38 Data Output Timing Parameter Values.	Rey de Luna	Oct 21, 2025
Draft 0.4	• Corrected Fig. 4-12 error that showed 5 warmup cycles in 8-4-2-1 Progressive Warmup Cycle for Read/Write Example diagram instead of 4 warmup cycles	Rey de Luna	Nov 04, 2025
Final	• Under section 3.3.1, added “(Optional)” description to section title • Under section 3.3.2 added “(Optional)” description to section title and modified 3rd paragraph from "It is NAND vendor specific whether a device supports one, both, or none of the above ..." to "It is NAND vendor specific whether a device supports one or both of the above ..."	Rey de Luna	Dec 18, 2025

Table of Contents

Table of Figures

Table of Tables

1. Introduction

1.1. Goals and Objectives

This specification defines a standardized NAND Flash device interface that provides the means for a system to be designed that supports a range of NAND Flash devices without direct design pre-association. The solution also provides the means for a system to seamlessly make use of new NAND devices that may not have existed at the time that the system was designed.

ONFI6.0 provides a standardized definition for the 4800MT/s data rate NAND interface and includes changes from the past ONFI 5.2 revision (SCA Protocol and ONFI 5.2 errata).

Legacy functionality and form factors that are no longer seen being supported on 4800MT/s capable NAND devices have been removed from the specification, including:

- Definitions and specifications for legacy interfaces: SDR, NV-DDR, NV-DDR2 and NV-DDR3
- Definitions for legacy packages: TSOP-48, LGA-52, BGA-63, BGA-100
- Behavioral flows for standard brevity moving forward

Please refer to older ONFI spec revisions on the ONFI website https://www.onfi.org for information related to these legacy features, form factors and behavioral flows.

1.2. References

The specification references the following specifications and standards:

- JEDEC JESD230G.01 standard. Standard is available at http://www.jedec.org.

1.3. Definitions, abbreviations, and conventions

1.3.1. Definitions and Abbreviations

The terminology used in this specification is intended to be self-sufficient and does not rely on overloaded meanings defined in other specifications. Terms with specific meaning not directly clear from the context are clarified in the following sections.

1.3.1.1. address

The address is comprised of a row address and a column address. The row address identifies the page, block, and LUN to be accessed. The column address identifies the byte or word within a page to access. The least significant bit of the column address shall always be zero.

1.3.1.2. asynchronous

Asynchronous is when data is latched with the WE_n signal for writes and RE_n signal for reads.

1.3.1.3. block

Consists of multiple pages and is the smallest addressable unit for erase operations.

1.3.1.4. column

The byte (x8 devices) or word (x16 devices) location within the page register.

1.3.1.5. CTT

Acronym for Center Tap Termination. Refers to the NAND interface termination scheme which connects the ODT resistance only to V_{TT} (i.e., 0.5*VccQ). CTT may also refer to the NV-DDR3 interface which utilizes such a termination scheme.

1.3.1.6. data burst

A data burst is a continuous set of data input or data output cycles without a pause. Specifically, there is not more than a data cycle time of pause within the data sequence.

1.3.1.6.1. data burst end

The host issues a new command after exiting the data burst. This exits NAND read mode and ends the data burst.

1.3.1.6.2. data burst exit

The host brings CE_n, ALE or CLE high during the data burst. ODT is off (if enabled) when in exit state and warmup cycles are re-issued (if enabled) if the data burst is continued after exit.

1.3.1.6.3. data burst pause

The host stops DQS (input burst) or RE (output burst) during data burst. ODT (if enabled) stays enabled the entire pause time and warmup cycles (if enabled) are not re-issued when continuing the data burst from pause.

1.3.1.7. DBI

Acronym for Data Bus Inversion.

1.3.1.8. DDR

Acronym for double data rate.

1.3.1.9. defect area

The defect area is where factory defects are marked by the manufacturer. Refer to section 3.3.

1.3.1.10. Deselected (ODT state)

When on-die termination is used, the LUN may be in a Deselected, Selected, or Sniff state with associated actions for each. Refer to section 4.13.

1.3.1.11. device

The packaged NAND unit. A device consists of one or more NAND Targets.

1.3.1.12. DFE

Acronym for Decision Feedback Equalizer.

1.3.1.13. differential signaling

Differential signaling is a method of transmitting information by means of two complementary signals. The opposite technique is called single-ended signaling. The RE_n and DQS signals may each have complementary signals enabled to improve noise immunity.

1.3.1.14. Dword

A Dword is thirty-two (32) bits of data. A Dword may be represented as 32 bits, as two adjacent words, or as four adjacent bytes. When shown as bits the least significant bit is bit 0 and most significant bit is bit 31. The most significant bit is shown on the left. When shown as words the least significant word (lower) is word 0 and the most significant (upper) word is word 1. When shown as bytes the least significant byte is byte 0 and the most significant byte is byte 3. See Figure 1 for a description of the relationship between bytes, words, and Dwords.

1.3.1.15. Host Target

A set of NAND Targets that share the same host CE_n signal. If CE_n reduction is not used, then a Host Target is equivalent to a NAND Target.

1.3.1.16. latching edge

The latching edge describes the edge of the RE_n, WE_n, or DQS signal that the contents of the command/data bus are latched on.

For NV-LPDDR4 (with and without VccQL), the latching edge for data cycles is both the rising and falling edges of the DQS signal. For Conv. Protocol command and address cycles, the latching edge is the rising edge of the WE_n signal.

1.3.1.17. LTT

Acronym for Low Tap Termination. Refers to the NAND interface termination scheme which connects the ODT resistance to Vss. LTT may be used to refer to the NV-LPDDR4 interface which utilizes such a termination scheme.

1.3.1.18. LUN (logical unit number)

The minimum unit that can independently execute commands and report status. There are one or more LUNs per NAND Target.

1.3.1.19. na

na stands for “not applicable”. Fields marked as “na” are not used.

1.3.1.20. NAND Target

A set of LUNs that share one CE_n signal within one NAND package.

1.3.1.21. O/M

O/M stands for Optional/Mandatory requirement. When the entry is set to “M”, the item is mandatory. When the entry is set to “O”, the item is optional.

1.3.1.22. on-die termination (ODT)

On-die termination is a type of electrical termination where the termination is provided by the NAND device. On-die termination is commonly referred to by its acronym, ODT. Refer to section 4.13.

1.3.1.23. page

The smallest addressable unit for read and program operations.

1.3.1.24. page register

Register used to read data from that was transferred from the Flash array. For program operations, the data is placed in this register prior to transferring the data to the Flash array.

1.3.1.25. partial page (obsolete)

A portion of the page, referred to as a partial page, may be programmed if the NAND Target supports more than one program per page as indicated in the parameter page. The host may choose to read only a portion of the data from the page register in a read operation; this portion may also be referred to as a partial page.

1.3.1.26. PI-LTT

Acronym for Power Isolated Low Tap Termination. Refers to the NV-LPDDR4 interface variation which uses both VccQ and VccQL supplies. In this document, another term for PI-LTT is NV-LPDDR4 with VccQL.

1.3.1.27. read request

A read request is a data output cycle request from the host that results in a data transfer from the device to the host. Refer to section 4.2 for information on data output cycles.

1.3.1.28. RDCA

Acronym for Read Duty Cycle Adjustment.

1.3.1.29. row

Refers to the block and page to be accessed.

1.3.1.30. SCA

Acronym for Separate Command Address protocol.

1.3.1.31. Selected (ODT state)

When on-die termination is used, the LUN may be in a Deselected, Selected, or Sniff state with associated actions for each. Refer to section 4.13.

1.3.1.32. single-ended signaling

Single-ended signaling is when a one signal is used to transmit information. The opposite technique is differential signaling.

1.3.1.33. Sniff (ODT state)

When on-die termination is used, the LUN may be in a Deselected, Selected, or Sniff state with associated actions for each. Refer to section 4.13.

1.3.1.34. source synchronous

Source synchronous is when the strobe (DQS) is forwarded with the data to indicate when the data should be latched. The strobe signal, DQS, can be thought of as an additional data bus bit.

1.3.1.35. SR[ ]

SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN. Refer to section 6.13 for the definition of bit meanings within the status register.

1.3.1.36. target

This term is equivalent to a NAND Target. When there is no potential confusion between NAND Target and Host Target, the shorter term of “target” is used.

1.3.1.37. Uncorrectable Bit Error Rate, or ratio (UBER)

A metric for the rate of occurrence of data errors, equal to the number of data errors per bits read. Mathematically, it may be represented as:

UBER = cumulative number of data errors / cumulative number of bits read

Note: The cumulative number of bits read is the sum of all bits of data read back from the device, with multiple reads of the same memory bit as multiple bits read. For example, if a 100GB device is read ten times then there would be about 1TB ($8x10^{12}$ bits) read. The cumulative number of data errors is the count of the physical pages for which the device fails to return correct data.

1.3.1.38. Volume

Applies to Conv. Protocol only. A Volume is an appointed address to a NAND Target. Volumes are used as part of Volume addressing.

1.3.1.39. VREFQ

Input reference voltage.

1.3.1.40. WDCA

Acronym for Write Duty Cycle Adjustment.

1.3.1.41. word

A word is sixteen (16) bits of data. A word may be represented as 16 bits or as two adjacent bytes. When shown as bits the least significant bit is bit 0 and most significant bit is bit 15. The most significant bit is shown on the left. When shown as bytes the least significant byte (lower) is byte 0 and the most significant byte (upper) is byte 1. See Figure 1-1 for a description of the relationship between bytes, words and Dwords.

1.3.2. Conventions

The names of abbreviations and acronyms used as signal names are in all uppercase (e.g., CE_n). “_n” is used indicate an active low signal (i.e., an inverted logic sense). It is acceptable to use the overbar, trailing slash (\), or # symbol rather than “_n” to indicate an active low signal. “_t” is used to indicate the true signal and “_c” is used to indicate the complementary signal when using differential signaling for a signal pair (e.g., RE_n or DQS).

Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. Numerical fields are unsigned unless otherwise indicated.

1.3.2.1. Precedence

If there is a conflict between text, figures, state machines, timing diagrams, and tables, the precedence shall be state machines, timing diagrams, tables, figures, and then text.

1.3.2.2. Keywords

Several keywords are used to differentiate between different levels of requirements.

1.3.2.2.1. mandatory

A keyword indicating items to be implemented as defined by this specification.

1.3.2.2.2. may

A keyword that indicates flexibility of choice with no implied preference.

1.3.2.2.3. optional

A keyword that describes features that are not required by this specification. However, if any optional feature defined by the specification is implemented, the feature shall be implemented in the way defined by the specification.

1.3.2.2.4. reserved

A keyword indicating reserved bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, or field shall be cleared to zero, or in accordance with a future extension to this specification. The recipient shall not check reserved bits, bytes, words, or fields.

1.3.2.2.5. shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the specification.

1.3.2.2.6. should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

1.3.2.3. Byte, word and Dword Relationships

Figure 1-1 illustrates the relationship between bytes, words and Dwords.

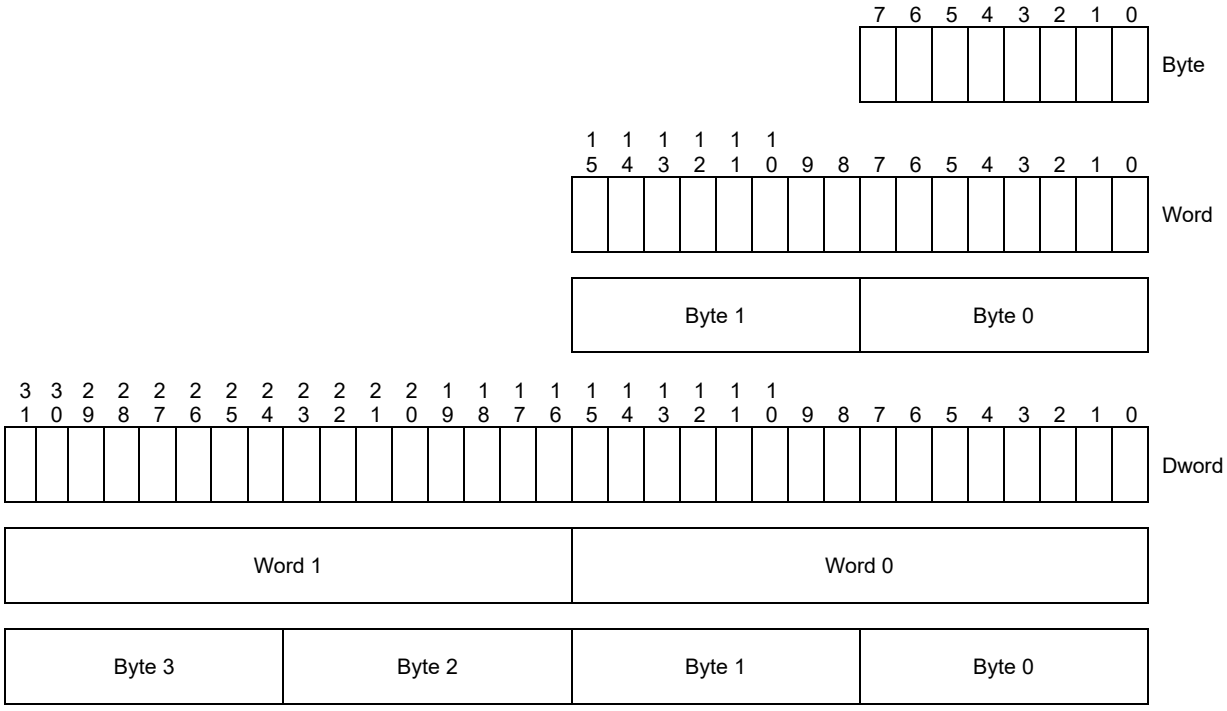


Figure 1-1 Byte, word and Dword Relationships

2. Physical Interface

2.1. BGA-152 and BGA-132 Ball Assignments

Figure 2-1 defines the ball assignments for devices using 152-ball BGA packaging with dual 8-bit data access. Figure 2-2 defines the ball assignments for devices using 132-ball BGA packaging with dual 8-bit data access. Figure 2-3 defines the ball spacing requirements for the 152-ball and 132-ball BGA package. There are two package sizes: 12mm x 18mm (132-ball) and 14mm x 18mm (152-ball). Note: If the 12mm x 18mm package size is used, then outer columns are not present, and the package is a 132-ball BGA. For the 132-ball BGA, the columns are re-enumerated to begin at column 1 (i.e. BGA-152 column 2 becomes BGA-132 column 1). Depending on the data interface selected, balls may have different usages and/or meanings. Refer to for the specific use for each ball in each data interface. ONFI does not support ODT pin. Ball-map showing ODT_*_n/WP_*_n muxing is just as a reference to JEDEC.

The conventional pins CE#, ALE, CLE, WE# maps to CA_CE#, CA[0], CA[1], CA_CLK respectively in SCA Protocol (See Separate Command Address (SCA) Protocol Section for more details).

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC	NC						NC	NC	NC	NC
B	NC	NC	NC	NC						NC	NC	NC	NC
C	NU	NU	NU	NU						NU	NU	NU	NU
D	NU	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU	NU
E	NU	NU	VSSQ	DQ2_1	VSSQ	DQS_1_t		RE_1_t (RE_1_n)	VSSQ	DQ5_1	VSSQ	NU	NU
F			DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n	VREFQ_ DNU	DQ6_1	DQ7_1		
G			VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ		
H			CE2_0_n or NU	CE3_0_n or NU	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	SCA_0 or NU		
J			VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS		
K			SCA_1 or NU	RZQ_0	CE0_0_n	CE1_0_n		Vpp or NU	WP_0_n or ODT_0_n	CE3_1_n or NU	CE2_1_n or NU		
L			VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ		
M			DQ7_0	DQ6_0	VREFQ_DNU	WE_0_n		RE_0_c	DQS_0_c	DQ1_0	DQ0_0		
N	NU	NU	VSSQ	DQ5_0	VSSQ	RE_0_t (RE_0_n)		DQS_0_t	VSSQ	DQ2_0	VSSQ	NU	NU
P	NU	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU	NU
R	NU	NU	NU	NU						NU	NU	NU	NU
T	NC	NC	NC	NC						NC	NC	NC	NC
U	NC	NC	NC	NC						NC	NC	NC	NC

Figure 2-1 BGA-152 ball assignments for dual 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC						NC	NC	NC
B	NC	NC	NC						NC	NC	NC
C	NU	NU	NU						NU	NU	NU
D	NU	VCCQ	VCCQ	DQ3_1	VSS		VCC	DQ4_1	VCCQ	VCCQ	NU
E	NU	VSSQ	DQ2_1	VSSQ	DQS_1_t		RE_1_t (RE_1_n)	VSSQ	DQ5_1	VSSQ	NU
F		DQ0_1	DQ1_1	DQS_1_c	RE_1_c		WE_1_n	VREFQ_ DNU	DQ6_1	DQ7_1	
G		VSSQ	VCCQ	ALE_1	CLE_1		DBI_1 or NU	VSSQ or NU	VCCQ	VSSQ	
H		CE2_0_n or NU	CE3_0_n or NU	WP_1_n or ODT_1_n	NU		CE1_1_n	CE0_1_n	RZQ_1	SCA_0 or NU	
J		VSS	VCC	R/B0_0_n	R/B1_0_n		R/B1_1_n	R/B0_1_n	VCC	VSS	
K		SCA_1 or NU	RZQ_0	CE0_0_n	CE1_0_n		Vpp or NU	WP_0_n or ODT_0_n	CE3_1_n or NU	CE2_1_n or NU	
L		VSSQ	VCCQ	VSSQ or NU	DBI_0 or NU		CLE_0	ALE_0	VCCQ	VSSQ	
M		DQ7_0	DQ6_0	VREFQ_DNU	WE_0_n		RE_0_c	DQS_0_c	DQ1_0	DQ0_0	
N	NU	VSSQ	DQ5_0	VSSQ	RE_0_t (RE_0_n)		DQS_0_t	VSSQ	DQ2_0	VSSQ	NU
P	NU	VCCQ	VCCQ	DQ4_0	VCC		VSS	DQ3_0	VCCQ	VCCQ	NU
R	NU	NU	NU						NU	NU	NU
T	NC	NC	NC						NC	NC	NC
U	NC	NC	NC						NC	NC	NC

Figure 2-2 BGA-132 ball assignments for dual 8-bit data access

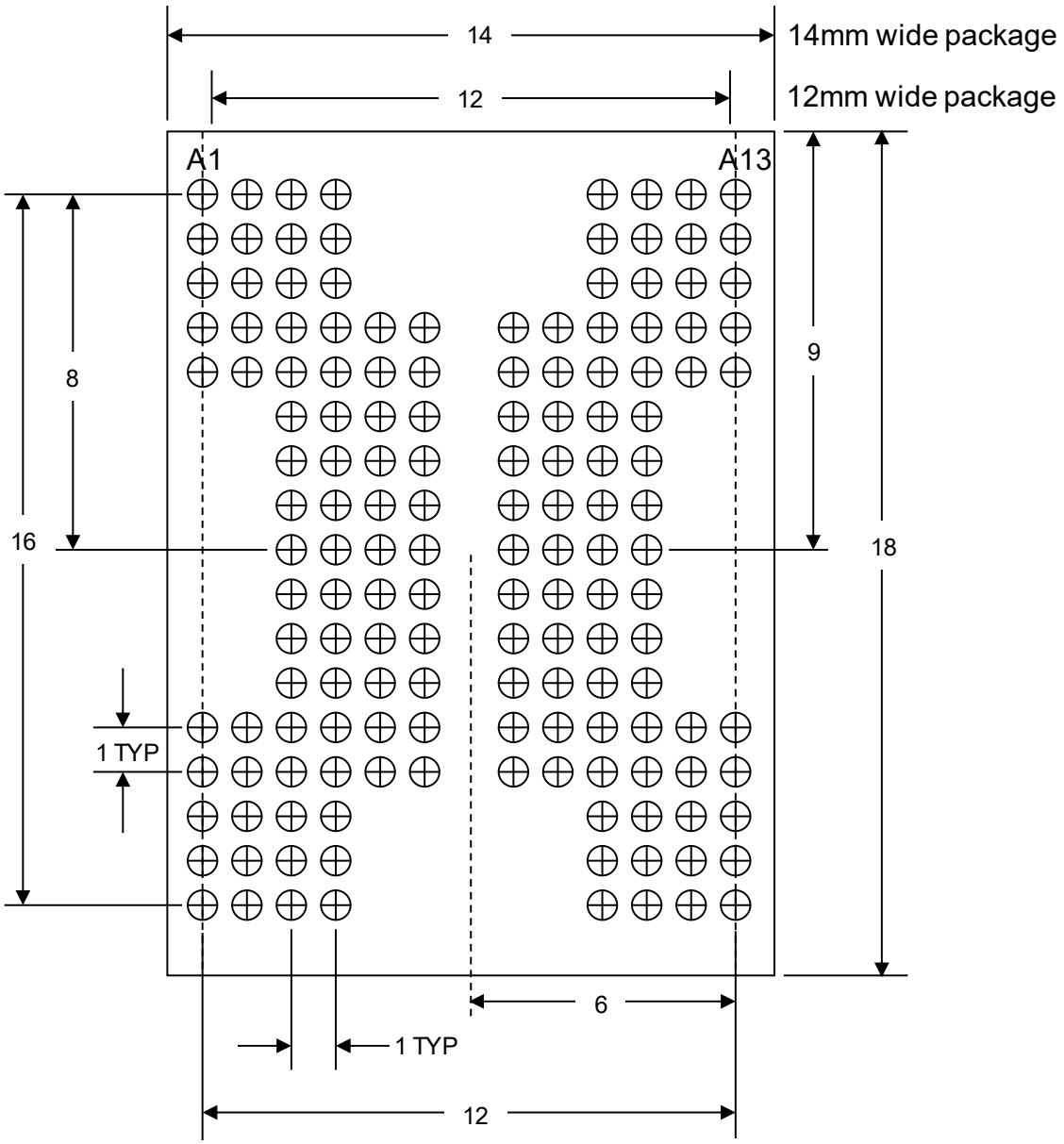


Figure 2-3 BGA-152 and BGA-132 ball spacing requirements (top view, dimensions in millimeters)

2.2. BGA-272, BGA-252, and BGA-316 Ball Assignments

Figure 2-4 defines the ball assignments for devices using 272-ball BGA packaging with quad 8-bit data access. Figure 2-5 defines the ball assignments for devices using 252-ball BGA packaging with quad 8-bit data access. Figure 2-6 defines the ball assignments for devices using 316-ball 16 CE_n BGA packaging with quad 8-bit data access. Figure 2-7 defines the ball assignments for devices using 316-ball 32 CE_n BGA packaging with quad 8-bit data access. Figure 2-8 defines the ball spacing requirements for the 272-ball and 252-ball BGA packages. Figure 2-9 defines the ball spacing requirements for the 316-ball BGA package. The package size for the 272-ball and 316-ball packages is 14mm x 18mm while the package size for the 252-ball package is 12mm x 18mm. The 252-ball package removes the outer columns from the 272-ball package resulting in a smaller package size. The 252-ball ball assignment is also re-enumerated to begin at column 1 (ie. BGA-272 column 2 becomes BGA-252 column 1). Depending on the data interface selected, balls may have different usages and/or meanings. Refer to for the specific use for each ball in each data interface. ONFI does not support ODT pin. Ball-map showing ODT_*_n/WP_*_n muxing is just as a reference to JEDEC.

The conventional pins CE#, ALE, CLE, WE# maps to CA_CE#, CA[0], CA[1], CA_CLK respectively in SCA Protocol (See Separate Command Address (SCA) Protocol Section for more details).

Balls labeled “VCCQ or VCCQL” in the ball assignments shall be connected to either VCCQ or VCCQL on the board and not be left floating.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NU									NU	NC	NC	NC
B	NC	NC	NU	VCCQ or VCCQL	VSS	VSS	VSS			VCC	VCCQ or VCCQL	VSS	VCCQ	NU	NC	NC
C	NC	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU	NC
D	NU	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC	NU
E	NU	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS	NU
F		VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VCCQ or VCCQL	
G		VCCQ or VCCQL	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ (TBD)	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ	
H		VCCQ	VSS	VSS	VSP0 or R	VSP2 or R or VCCQL	VSS			WE_0_n	CE1_0_n	CE3_0_n (TBD)	R/B0_0_n	R/B1_0_n	VSS	
J		NU	NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n	CE1_2_n	CE3_2_n	R/B0_2_n	R/B1_2_n	VSP6 or R	
K		VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_t (RE_0_n)	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4	VPP	
L		SCA_0 or NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_t (RE_2_n)	RE_2_c			VREFQ_DNU	VREFQ_DNU	VSS	VSS	VSS	VSS	
M		VSS	VSS	VSS	VSS	VREFQ_DNU	VREFQ_DNU			RE_3_c	RE_3_t (RE_3_n)	CLE_3	ALE_3	WP_3_n or ODT_3_n	SCA_1 or NU	
N		VPP	VSP5	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_t (RE_1_n)	CLE_1	ALE_1	WP_1_n or ODT_1_n	VCC	
P		VSP7 or R	R/B1_3_n	R/B0_3_n	CE3_3_n (TBD)	CE1_3_n	WE_3_n			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU	
R		VSS	R/B1_1_n	R/B0_1_n	CE3_1_n	CE1_1_n	WE_1_n			VSS	VSP3 or R or VCCQL	VSP1 or R	VSS	VSS	VCCQ	
T		VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ (TBD)			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VCCQ or VCCQL	
U		VCCQ or VCCQL	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS	
V	NU	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC	NU
W	NU	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC	NU
Y	NC	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU	NC
AA	NC	NC	NU	VCCQ	VSS	VCCQ or VCCQL	VCC			VSS	VSS	VSS	VCCQ or VCCQL	NU	NC	NC
AB	NC	NC	NC	NU									NU	NC	NC	NC

Figure 2-4 BGA-272 ball assignments for quad 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	NU									NU	NC	NC
B	NC	NU	VCCQ or VCCQL	VSS	VSS	VSS			VCC	VCCQ or VCCQL	VSS	VCCQ	NU	NC
C	NU	VCCQ	VSS	VSS	DQ0_2	DQ0_0			VSS	VSS	VSS	VSS	VCC	NU
D	VCC	VSS	VSS	VSS	DQ1_2	DQ1_0			DQ4_2	DQ4_0	VSS	VSS	VSS	VCC
E	VCC	VSS	VSS	VSS	DQ2_2	DQ2_0			DQ5_2	DQ5_0	VSS	VSS	VSS	VSS
F	VSS	VSS	VSS	DQ3_0	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			DQ6_2	DQ6_0	VSS	VSS	VSS	VCCQ or VCCQL
G	VCCQ or VCCQL	VSS	VSS	DQ3_2	DQS_2_c	DQS_0_c			VCCQ (TBD)	DQ7_2	DQ7_0	RZQ_2	RZQ_0	VCCQ
H	VCCQ	VSS	VSS	VSP0 or R	VSP2 or R or VCCQL	VSS			WE_0_n	CE1_0_n	CE3_0_n (TBD)	R/B0_0_n	R/B1_0_n	VSS
J	NU	NU	VSS	VSS	DBI_2 or NU	DBI_0 or NU			WE_2_n	CE1_2_n	CE3_2_n	R/B0_2_n	R/B1_2_n	VSP6 or R
K	VCC	WP_0_n or ODT_0_n	ALE_0	CLE_0	RE_0_t (RE_0_n)	RE_0_c			CE0_2_n	CE0_0_n	CE2_2_n	CE2_0_n	VSP4	VPP
L	SCA_0 or NU	WP_2_n or ODT_2_n	ALE_2	CLE_2	RE_2_t (RE_2_n)	RE_2_c			VREFQ_DNU	VREFQ_DNU	VSS	VSS	VSS	VSS
M	VSS	VSS	VSS	VSS	VREFQ_DNU	VREFQ_DNU			RE_3_c	RE_3_t (RE_3_n)	CLE_3	ALE_3	WP_3_n or ODT_3_n	SCA_1 or NU
N	VPP	VSP5	CE2_1_n	CE2_3_n	CE0_1_n	CE0_3_n			RE_1_c	RE_1_t (RE_1_n)	CLE_1	ALE_1	WP_1_n or ODT_1_n	VCC
P	VSP7 or R	R/B1_3_n	R/B0_3_n	CE3_3_n (TBD)	CE1_3_n	WE_3_n			DBI_1 or NU	DBI_3 or NU	VSS	VSS	NU	NU
R	VSS	R/B1_1_n	R/B0_1_n	CE3_1_n	CE1_1_n	WE_1_n			VSS	VSP3 or R or VCCQL	VSP1 or R	VSS	VSS	VCCQ
T	VCCQ	RZQ_1	RZQ_3	DQ7_1	DQ7_3	VCCQ (TBD)			DQS_1_c	DQS_3_c	DQ3_3	VSS	VSS	VCCQ or VCCQL
U	VCCQ or VCCQL	VSS	VSS	VSS	DQ6_1	DQ6_3			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	DQ3_1	VSS	VSS	VSS
V	VSS	VSS	VSS	VSS	DQ5_1	DQ5_3			DQ2_1	DQ2_3	VSS	VSS	VSS	VCC
W	VCC	VSS	VSS	VSS	DQ4_1	DQ4_3			DQ1_1	DQ1_3	VSS	VSS	VSS	VCC
Y	NU	VCC	VSS	VSS	VSS	VSS			DQ0_1	DQ0_3	VSS	VSS	VCCQ	NU
AA	NC	NU	VCCQ	VSS	VCCQ or VCCQL	VCC			VSS	VSS	VSS	VCCQ or VCCQL	NU	NC
AB	NC	NC	NU									NU	NC	NC

Figure 2-5 BGA-252 ball assignments for quad 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQ or VCCQL	VSS	VREFQ_DNU	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQ or VCCQL	VSS	NU	NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQ or VCCQL	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B_2_n	RZQ_2	VSS	VSS	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B_0_n	RZQ_0	VSS	VSS	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_n or ODT_2_n	CE1_2_n	CE3_2_n or VCCQL	VSS	VCC	NC
H	NC	VCC	VSS	VCCQ or VCCQL	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n or VCCQ	VSS	~~SCA_1~~ SCA_0 or NU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	VSS	VSS	NC
K	NC	VCCQ or VCCQL	VSS	VSS	DQ2_2	DQ2_0	RE_2_t (RE_2_n)			RE_0_t (RE_0_n)	ALE_0	CE0_0_n	CE2_0_n	VSS	VCC	NC
L	NC	NU	VREFQ_DNU	VSP	DQ1_2	DQ1_0	WE_2_n			WE_0_n	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n			WE_3_n	DQ1_1	DQ1_3	VSP	VREFQ_DNU	NU	NC
N	NC	VCC	VSS	CE2_1_n	CE0_1_n	ALE_1	RE_1_t (RE_1_n)			RE_3_t (RE_3_n)	DQ2_1	DQ2_3	VSS	VSS	VCCQ or VCCQL	NC
P	NC	VSS	VSS	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	~~SCA_0~~ SCA_1 or NU	VSS	CE3_1_n or VCCQ	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQ or VCCQL	VSS	VCC	NC
T	NC	VCC	VSS	CE3_3_n or VCCQL	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	VSS	VSS	RZQ_1	R/B_1_n	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	VSS	VSS	RZQ_3	R/B_3_n	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQ or VCCQL	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQ or VCCQL			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREFQ_DNU	VSS	VCCQ or VCCQL	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 2-6 BGA-316 ball 16 CE_n assignments for quad 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	VCCQ	VSS	VCCQ or VCCQL	VSS	VRE FQ_ DNU	VCC	VSS	VCC	VSS	VCC	NC	NC	NC
C	NC	NC	VSS	VCC	VSS	DQ7_2	DQ7_0			VCCQ or VCCQL	VSS	NU	NU	VPP	NC	NC
D	NC	VCC	VSS	VSP	VSP	DQ6_2	DQ6_0			VSS	VSS	VSS	VSS	VSS	VCC	NC
E	NC	VCCQ or VCCQL	VSS	VSP	VSP	DQ5_2	DQ5_0			DBI_2 or NU	R/B_2_n	RZQ_2	CE6_2_n	CE7_2_n	RFU	NC
F	NC	VSS	VSS	VCCQ	VSS	DQ4_2	DQ4_0			DBI_0 or NU	R/B_0_n	RZQ_0	CE6_0_n	CE7_0_n	VSS	NC
G	NC	VCCQ	VSS	VCC	VSS	DQS_2 (DQS_2_t)	DQS_0 (DQS_0_t)			WP_0_n or ODT_0_n	WP_2_nor ODT_2_n	CE1_2_n	CE3_2_n or VccQL	CE5_2_n	VCC	NC
H	NC	VCC	VSS	VCCQ or VCCQL	VSS	DQS_2_c	DQS_0_c			CLE_0	CLE_2	CE1_0_n	CE3_0_n or VccQ	CE5_0_n	~~SCA_1~~ SCA_0 or NU	NC
J	NC	VSP	VSP	VSS	DQ3_2	DQ3_0	RE_2_c			RE_0_c	ALE_2	CE0_2_n	CE2_2_n	CE4_2_n	VSS	NC
K	NC	VCCQ or VCCQL	VSS	VSS	DQ2_2	DQ2_0	RE_2_t (RE_2_n)			RE_0_t (RE_0_n)	ALE_0	CE0_0_n	CE2_0_n	CE4_0_n	VCC	NC
L	NC	NU	VREFQ _DNU	VSP	DQ1_2	DQ1_0	WE_2_n			WE_0_n	DQ0_1	DQ0_3	VSP	VSS	VCCQ	NC
M	NC	VCCQ	VSS	VSP	DQ0_2	DQ0_0	WE_1_n			WE_3_n	DQ1_1	DQ1_3	VSP	VREFQ _DNU	NU	NC
N	NC	VCC	CE4_1_n	CE2_1_n	CE0_1_n	ALE_1	RE_1_t (RE_1_n)			RE_3_t (RE_3_n)	DQ2_1	DQ2_3	VSS	VSS	VCCQ or VCCQL	NC
P	NC	VSS	CE4_3_n	CE2_3_n	CE0_3_n	ALE_3	RE_1_c			RE_3_c	DQ3_1	DQ3_3	VSS	VSP	VSP	NC
R	NC	~~SCA_0~~ SCA_1 or NU	CE5_1_n	CE3_1_n or VccQ	CE1_1_n	CLE_3	CLE_1			DQS_1_c	DQS_3_c	VSS	VCCQ or VCCQL	VSS	VCC	NC
T	NC	VCC	CE5_3_n	CE3_3_n or VccQL	CE1_3_n	WP_3_n or ODT_3_n	WP_1_n or ODT_1_n			DQS_1 (DQS_1_t)	DQS_3 (DQS_3_t)	VSS	VCC	VSS	VCCQ	NC
U	NC	VSS	CE7_1_n	CE6_1_n	RZQ_1	R/B_1_n	DBI_1 or NU			DQ4_1	DQ4_3	VSS	VCCQ	VSS	VSS	NC
V	NC	RFU	CE7_3_n	CE6_3_n	RZQ_3	R/B_3_n	DBI_3 or NU			DQ5_1	DQ5_3	VSP	VSP	VSS	VCCQ or VCCQL	NC
W	NC	VCC	VSS	VSS	VSS	VSS	VSS			DQ6_1	DQ6_3	VSP	VSP	VSS	VCC	NC
Y	NC	NC	VPP	RFU	RFU	VSS	VCCQ or VCCQL			DQ7_1	DQ7_3	VSS	VCC	VSS	NC	NC
AA	NC	NC	NC	VCC	VSS	VCC	VSS	VCC	VREF Q_DNU	VSS	VCCQ or VCCQL	VSS	VCCQ	NC	NC	NC
AB	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

Figure 2-7 BGA-316 ball 32 CE_n assignments for quad 8-bit data access

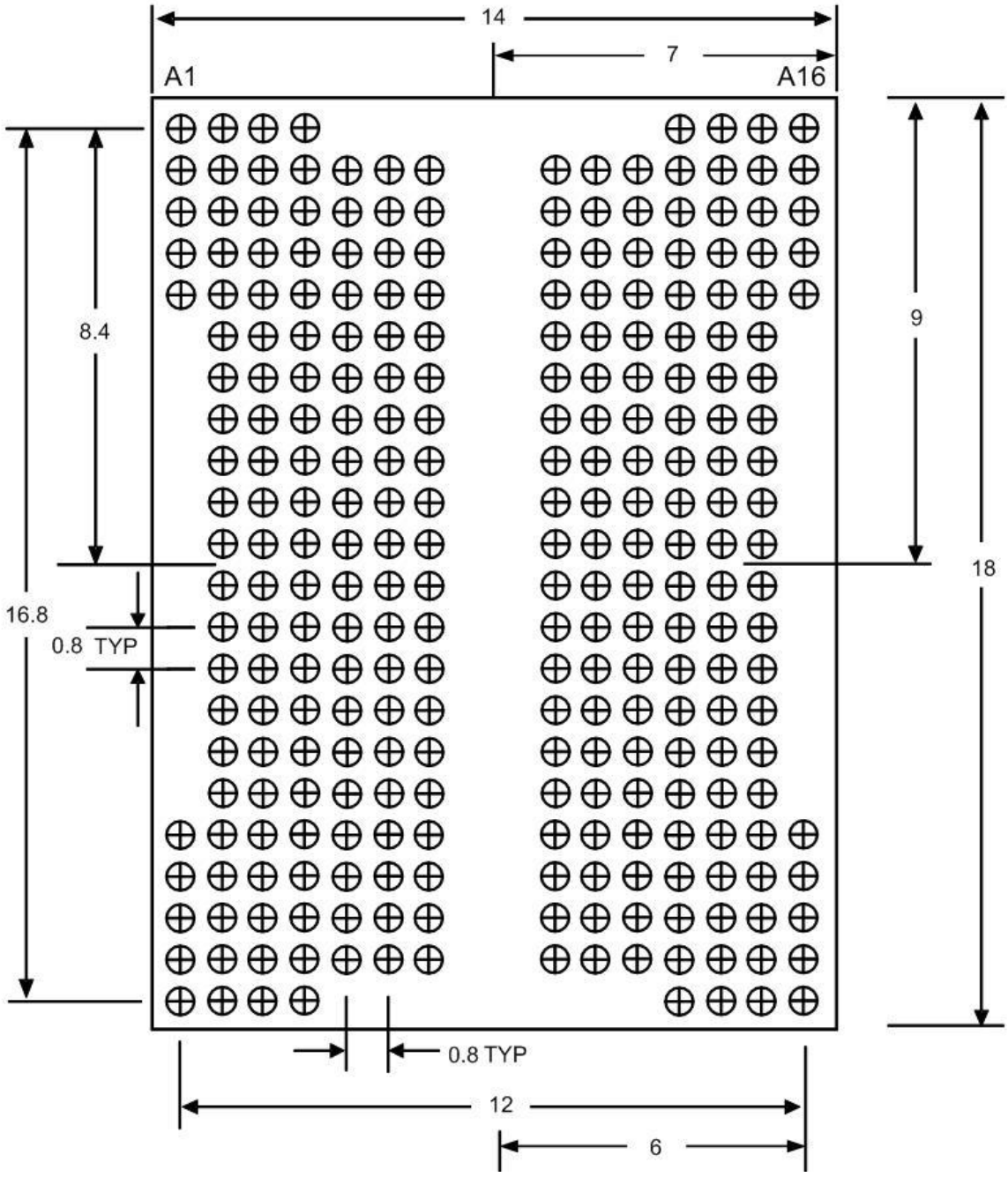


Figure 2-8 BGA-272 and BGA-252 ball spacing requirements (top view, dimensions in millimeters)

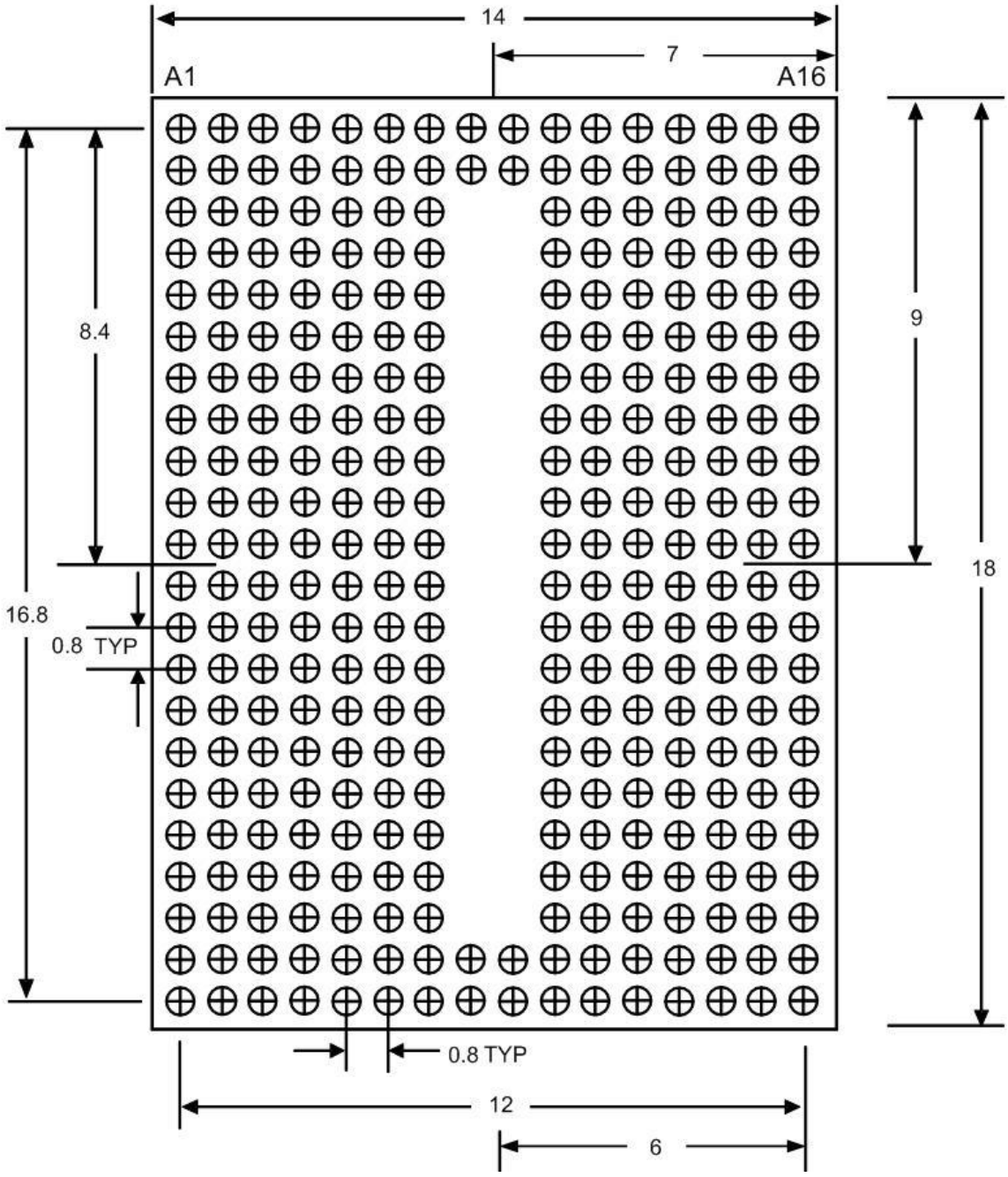


Figure 2-9 BGA-316 ball spacing requirements (top view, dimensions in millimeters)

2.3. BGA-178, BGA-154, and BGA-146 Ball Assignments

Figure 2-10 defines the ball assignments for devices using 178-ball BGA packaging with dual 8-bit data access. Figure 2-11 defines the ball assignments for devices using 154-ball BGA packaging with dual 8-bit data access. Figure 2-12 defines the ball assignments for devices using 146-ball BGA packaging with dual 8-bit data access. Figure 2-13, Figure 2-14, Figure 2-15 define the ball spacing requirements for the 178-ball, 154-ball and 146-ball BGA packages. The package size for the 178-ball package is 13.5mm x 13.5mm. The package size for the 154-ball package is either 11.5x13.5mm or 12.8x13.5 mm. The package size for the 146-ball package is either 10x18mm or 10x14mm. The 154-ball package removes the outer columns from the 178-ball package resulting in a smaller package size. The 154-ball package ball assignment is also re-enumerated to begin at column 1 (i.e. BGA-178 column 2 becomes BGA-154 column 1). The 146-ball package transposes the rows and columns from the 178-ball package and removes the 2 outer columns on each side. The 146-ball package ball assignment is also re-enumerated to begin at column 1 (i.e. BGA-178 row N becomes BGA-146 column 1). Depending on the data interface selected, balls may have different usages and/or meanings. Refer to for the specific use for each ball in each data interface. ONFI does not support ODT pin. Ball-map showing ODT_*_n/WP_*_n muxing is just as a reference to JEDEC.

The conventional pins CE#, ALE, CLE, WE# maps to CA_CE#, CA[0], CA[1], CA_CLK respectively in SCA Protocol (See Separate Command Address (SCA) Protocol Section for more details).

Balls labeled “VCCQ or VCCQL” in the ball assignments shall be connected to either VCCQ or VCCQL on the board and not be left floating.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	NC	NC								NC	NC	NC	NC
B	NC	NU	NU	NU								NU	NU	NU	NC
C	NC	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU	NC
D	NC	NU	VCCQ	VCC	RFU	VPP	ZQ_0	VREFQ _DNU	SCA_1 or NU	VSP	VSP	VCC	VCCQ	NU	NC
E	NC	NU	VSS	DQ5_0	VCCQ or VCCQL	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VCCQ or VCCQL	DQ2_1	VSS	NU	NC
F	NC	NU	VCCQ or VCCQL	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VCCQ or VCQL	NU	NC
G		NU	VCC	RE_0_t (RE_0_n)	RE_0_c	WE_0_n	CE3_0_n or VCCQ	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU	
H															
J		NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n or VCCQ	WE_1_n	RE_1_c	RE_1_t (RE_1_n)	VCC	NU	
K	NC	NU	VCCQ or VCCQL	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VCCQ or VCCQL	NU	NC
L	NC	NU	VSS	DQ2_0	VCCQ or VCCQL	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VCCQ or VCCQL	DQ5_1	VSS	NU	NC
M	NC	NU	VCCQ	VCC	VSP	VSP	SCA_0 or NU	VREFQ _DNU	ZQ_1	VPP	RFU	VCC	VCCQ	NU	NC
N	NC	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU	NC
P	NC	NU	NU	NU								NU	NU	NU	NC
R	NC	NC	NC	NC								NC	NC	NC	NC

Figure 2-10 BGA-178 ball assignments for dual 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	NC	NC								NC	NC	NC
B	NU	NU	NU								NU	NU	NU
C	NU	NU	VCCQ	VSS	VPP	VSS	VCC	VSS	VCCQ	VSS	VCCQ	NU	NU
D	NU	VCCQ	VCC	RFU	VPP	ZQ_0	VREFQ _DNU	SCA_1 or NU	VSP	VSP	VCC	VCCQ	NU
E	NU	VSS	DQ5_0	VCCQ or VCCQL	DQ7_0	CE1_0_n	CE0_0_n	WP_1_n ODT_1_n	DQ0_1	VCCQ or VCCQL	DQ2_1	VSS	NU
F	NU	VCCQ or VCCQL	DQ4_0	VSS	DQ6_0	CE2_0_n	R/B0_0_n	ALE_1	DQ1_1	VSS	DQ3_1	VCCQ or VCCQL	NU
G	NU	VCC	RE_0_t (RE_0_n)	RE_0_c	WE_0_n	CE3_0_n or VCCQ	R/B1_0_n	CLE_1	DBI_1 or NU	DQS_1_c	DQS_1_t	VSS	NU
H													
J	NU	VSS	DQS_0_t	DQS_0_c	DBI_0 or NU	CLE_0	R/B1_1_n	CE3_1_n or VCCQ	WE_1_n	RE_1_c	RE_1_t (RE_1_n)	VCC	NU
K	NU	VCCQ or VCCQL	DQ3_0	VSS	DQ1_0	ALE_0	R/B0_1_n	CE2_1_n	DQ6_1	VSS	DQ4_1	VCCQ or VCCQL	NU
L	NU	VSS	DQ2_0	VCCQ or VCCQL	DQ0_0	WP_0_n ODT_0_n	CE0_1_n	CE1_1_n	DQ7_1	VCCQ or VCCQL	DQ5_1	VSS	NU
M	NU	VCCQ	VCC	VSP	VSP	SCA_0 or NU	VREFQ _DNU	ZQ_1	VPP	RFU	VCC	VCCQ	NU
N	NU	NU	VCCQ	VSS	VCCQ	VSS	VCC	VSS	VPP	VSS	VCCQ	NU	NU
P	NU	NU	NU								NU	NU	NU
R	NC	NC	NC								NC	NC	NC

Figure 2-11 BGA-154 ball assignments for dual 8-bit data access

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	NC	NC				NC	NC	NC	NC
B	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
C	NU	VCCQ	VSS	VCCQ or VCCQL	VSS		VCC	VCCQ or VCCQL	VSS	VCCQ	NU
D	VCCQ	VCC	DQ2_0	DQ3_0	DQS_0_t		RE_0_t (RE_0_n)	DQ4_0	DQ5_0	VCC	VCCQ
E	VSS	VSP	VCCQ or VCCQL	VSS	DQS_0_c		RE_0_c	VSS	VCCQ or VCCQL	RFU	VSS
F	VCCQ	VSP	DQ0_0	DQ1_0	DBI_0 or NU		WE_0_n	DQ6_0	DQ7_0	VPP	VPP
G	VSS	SCA_0 or NU	WP_0_n ODT_0_n	ALE_0	CLE_0		CE3_0_n or VCCQ	CE2_0_n	CE1_0_n	ZQ_0	VSS
H	VCC	VREFQ _DNU	CE0_1_n	R/B0_1_n	R/B1_1_n		R/B1_0_n	R/B0_0_n	CE0_0_n	VREFQ _DNU	VCC
J	VSS	ZQ_1	CE1_1_n	CE2_1_n	CE3_1_n or VCCQ		CLE_1	ALE_1	WP_1_n ODT_1_n	SCA_1 or NU	VSS
K	VPP	VPP	DQ7_1	DQ6_1	WE_1_n		DBI_1 or NU	DQ1_1	DQ0_1	VSP	VCCQ
L	VSS	RFU	VCCQ or VCCQL	VSS	RE_1_c		DQS_1_c	VSS	VCCQ or VCCQL	VSP	VSS
M	VCCQ	VCC	DQ5_1	DQ4_1	RE_1_t (RE_1_n)		DQS_1_t	DQ3_1	DQ2_1	VCC	VCCQ
N	NU	VCCQ	VSS	VCCQ or VCCQL	VCC		VSS	VCCQ or VCCQL	VSS	VCCQ	NU
P	NU	NU	NU	NU	NU		NU	NU	NU	NU	NU
R	NC	NC	NC	NC				NC	NC	NC	NC

Figure 2-12 BGA-146 ball assignments for dual 8-bit data access

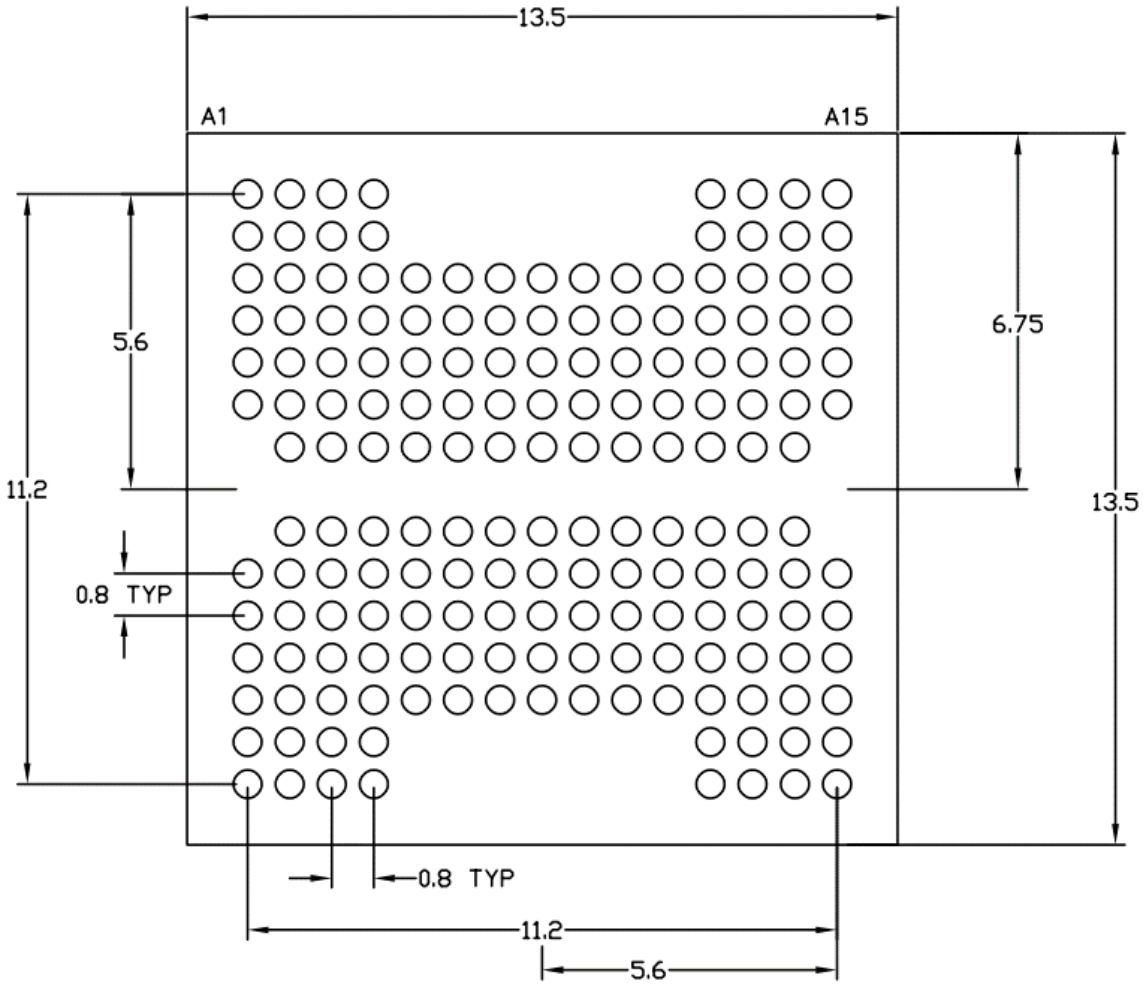


Figure 2-13 BGA-178 ball spacing requirements (top view, dimensions in millimeters)

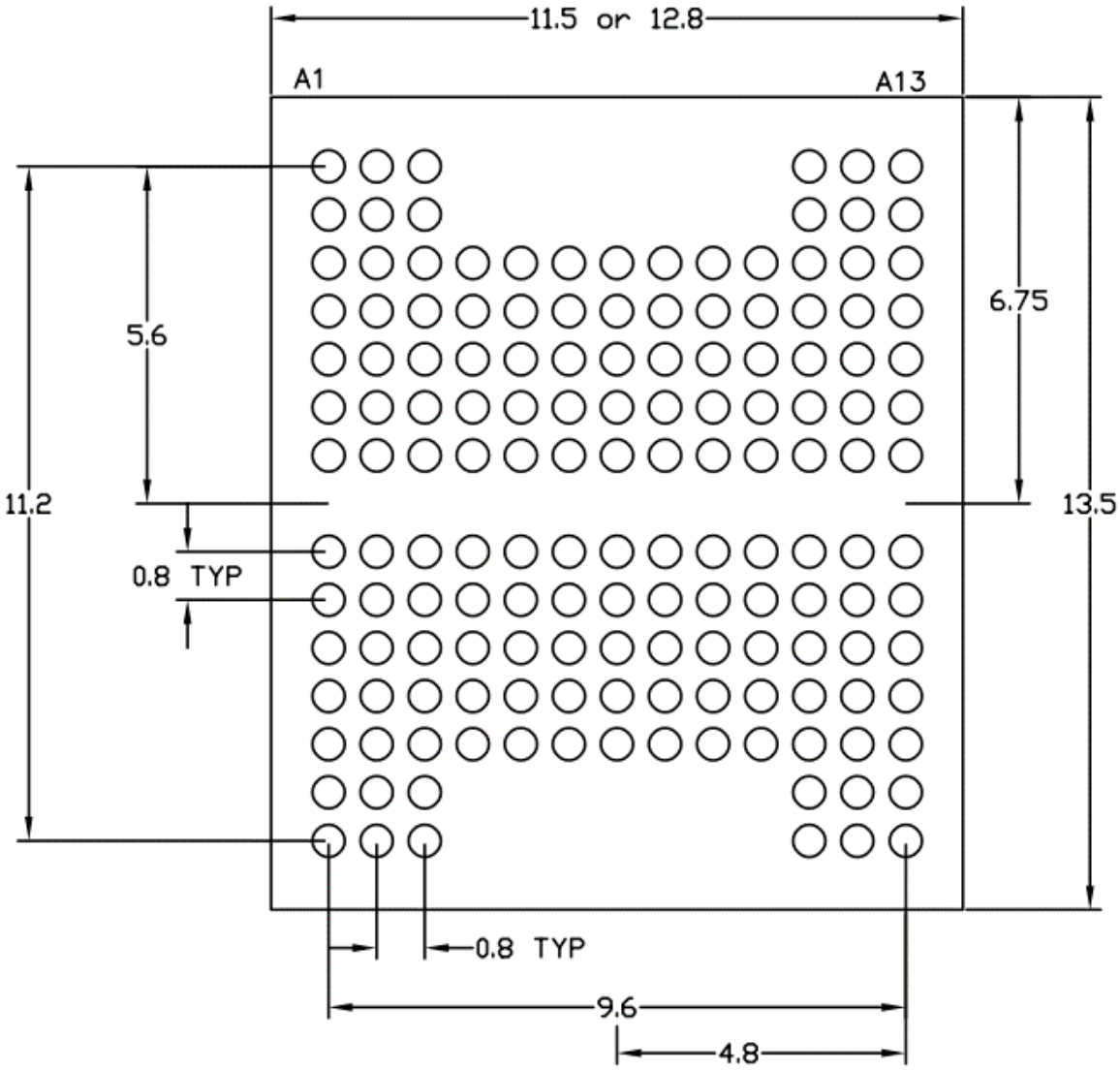


Figure 2-14 BGA-154 ball spacing requirements (top view, dimensions in millimeters)

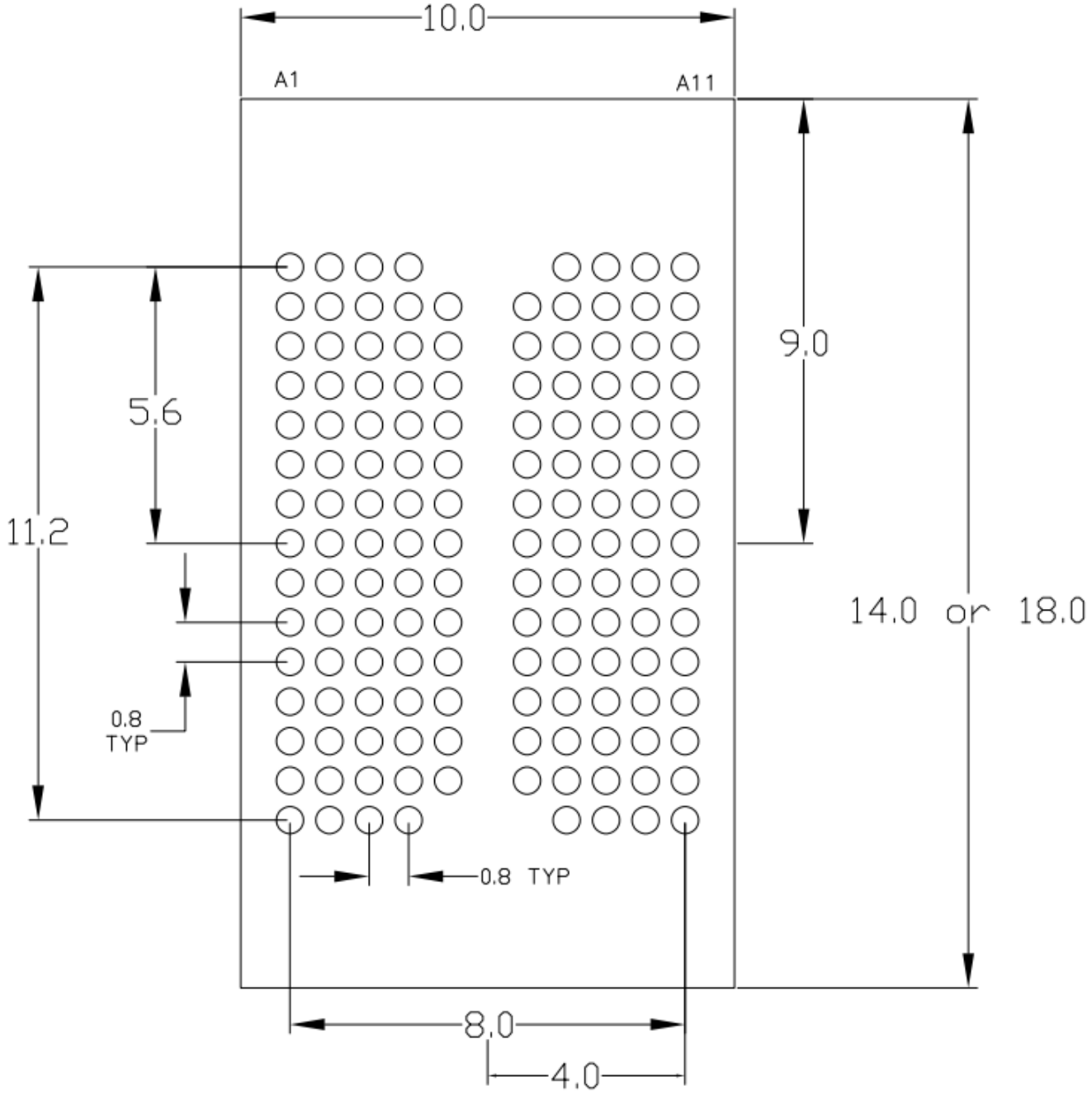


Figure 2-15 BGA-146 ball spacing requirements (top view, dimensions in millimeters)

2.4. Signal Descriptions

Table 2-1 provides the Conventional Protocol signal descriptions.

Signal Name	Input / Output	Description
R/By_x_n	O	**Ready/Busy** The Ready/Busy signal indicates the target status. When low, the signal indicates that one or more LUN operations are in progress. This signal is an open drain output and requires an external pull-up.
RE_x_t (RE_x_n)	I	**Read Enable (True)** The Read Enable (True) signal enables serial data output.
RE_x_c	I	**Read Enable Complement** The Read Enable Complement signal is the complementary signal to Read Enable True. Specifically, Read Enable Complement has the opposite value of Read Enable True when CE_n is low, i.e., if RE_x_t is high then RE_x_c is low; if RE_x_t is low then RE_x_c is high. Read Enable Complement signal is required to be used on the NV-LPDDR4 interface regardless of data rate.
CEy_x_n	I	**Chip Enable** The Chip Enable signal selects the target. When Chip Enable is high and the target is in the ready state, the target goes into a low-power standby state. When Chip Enable is low, the target is selected.
Vcc	I	**Power** Vcc is the power supply to the device.
VccQ	I	**I/O Power** VccQ is the power supply for input and/or output signals.
VccQL	I	**I/O Power** VccQL is the power supply for input and/or output signals when NV-LPDDR4 with VccQL (PI-LTT) is enabled.
Vss	I	**Ground** The Vss signal is the power supply ground.
VssQ	I	**I/O Ground** The VssQ signal is the ground for input and/or output signals.
VREFQ_DNU	I	**Voltage Reference** VREFQ Do Not Use (DNU). External voltage reference optionally used on or older NAND devices but not used starting ONFI 6.0 NAND devices. This signal is a placeholder of the ball location of external VREFQ on the package ball map to prevent the balls from being used inadvertently for other purposes.
Vpp	I	**High Voltage Power** Vpp is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g., improved power efficiency).
CLE_x	I	**Command Latch Enable** The Command Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).
ALE_x	I	**Address Latch Enable** The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).

Signal Name	Input / Output	Description
WE_x_n	I	**Write Enable** The Write Enable signal controls the latching of commands and addresses. Commands and addresses are latched on the rising edge of WE_x_n.
WP_x_n	I	**Write Protect** The Write Protect signal disables Flash array program and erase operations.
IO0_x – IO7_x (DQ0_x – DQ7_x)	I/O	**I/O Port x, bits 0-7** The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device. Also known as DQ0_x – DQ7_x.
DQS (DQS_x_t)	I/O	**Data Strobe (True)** Bidirectional data strobe signal that indicates the data valid window.
DBI_x	I/O	**Data Bus Inversion** The is an optional function for NAND device to designate if the DQ signals are inverted by transmitter side or not.
DQS_x_c	I/O	**Data Strobe Complement** The Data Strobe Complement signal is the complementary signal to Data Strobe True. Specifically, Data Strobe Complement has the opposite value of Data Strobe True when CE_n is low, i.e. if DQS_x_t is high then DQS_x_c is low; if DQS_x_t is low then DQS_x_c is high. Data Strobe Complement signal is required to be used on the NV-LPDDR4 interface regardless of data rate.
VSP_x		**Vendor Specific** The function of these signals is defined and specified by the NAND vendor. Devices shall have an internal pull-up or pull-down resistor on these signals to yield ONFI compliant behavior when a signal is not connected by the host. Any VSP signal not used by the NAND vendor shall not be connected internal to the device. The VSP signals shall be treated as NU signals by the user.
R		**Reserved** These pins shall not be connected by the host.
RFT		**Reserved for Test** These pins shall not be connected by the host.
NU		**Not Usable** A pin that is not to be used in normal applications and that may or may not have an internal connection.
NC		**No (internal) Connection** A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.
ZQ_x	na	**Reference pin for ZQ calibration** This is used on ZQ calibration and ZQ signal shall be connected to Vss through RZQ resistor

Table 2-1 Conventional Protocol Signal Descriptions

Table 2-2 provides the SCA Protocol signal descriptions.

Signal Name	Input / Output	Description
CA[1:0]_x	I/O	**COMMAND/ADDRESS PACKET** CA bus signals control the command/address packet type according to the SCA header definition table.
CA_CEy_x_n	I	**COMMAND/ADDRESS BUS ENABLE** The CA_CEy_x_n input enables the CA bus for the LUNs connected to that CA_CEy_x_n. When CA_CEy_x_n is low, the target CA bus is selected. When CA_CEy_x_n is high and the target is in the ready state, the target goes into a low-power standby state. When CA_CEy_x_n is high in the middle of a CA packet transaction, the packet transaction is aborted and the LUNs on the CA_CEy_x_n restart their command pointers. The number after the first underscore represents the channel. For example, CE0_0_n indicates CE0_n of channel-0 and CE0_1_n does CE0_n of channel-1.
CA_CLK_x	I	**COMMAND/ADDRESS CLOCK** The CA_CLK_x signal is a clock input. The CA bus signals are latched on the rising and falling edges of the CA_CLK_x pulse. The CA_CLK_x signal is default LOW while WE_x_n signal in the conventional protocol is default HIGH.
DBI_x	I/O	**Data Bus Inversion** The is an optional function for NAND device to designate if the DQ signals are inverted by transmitter side or not.
DQS (DQS_x_t)	I/O	**Data Strobe (True)** Bidirectional data strobe signal that indicates the data valid window.
DQS_x_c	I/O	**Data Strobe Complement** The Data Strobe Complement signal is the complementary signal to Data Strobe True. Specifically, Data Strobe Complement has the opposite value of Data Strobe True when CE_n is low, i.e. if DQS_x_t is high then DQS_x_c is low; if DQS_x_t is low then DQS_x_c is high. Data Strobe Complement signal is required to be used on the NV-LPDDR4 interface regardless of data rate.
IO0_x – IO7_x (DQ0_x – DQ7_x)	I/O	**I/O Port x, bits 0-7** The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device. Also known as DQ0_x – DQ7_x.
NC		**No (internal) connection** A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.
NU		**Not Usable** A pin that is not to be used in normal applications and that may or may not have an internal connection.
RE_x_t (RE_x_n)	I	**Read Enable (True)** The Read Enable (True) signal enables serial data output.

Signal Name	Input / Output	Description
RE_x_c	I	**Read Enable Complement** The Read Enable Complement signal is the complementary signal to Read Enable True. Specifically, Read Enable Complement has the opposite value of Read Enable True when CE_n is low, i.e., if RE_x_t is high then RE_x_c is low; if RE_x_t is low then RE_x_c is high. Read Enable Complement signal is required to be used on the NV-LPDDR4 interface regardless of data rate.
R		**Reserved** These pins shall not be connected by the host.
RFT		**Reserved for Test** These pins shall not be connected by the host.
R/By_x_n	O	**Ready/Busy** The Ready/Busy signal indicates the target status. When low, the signal indicates that one or more LUN operations are in progress. This signal is an open drain output and requires an external pull-up.
SCA_x	I	Separate Command Address (SCA) protocol enable: enables or disables the protocol. When the SCA signal is Float or connected to Vss during power-up, the Conv. protocol is enabled. When the SCA signal is connected to VccQ during power-up, the SCA protocol is enabled. On a packaged device, all SCA balls on the package must be connected to the same value on the board (i.e. all SCA balls on the package connected to Vss, or all SCA balls on the package connected to VccQ, or all SCA balls on the package left Floating).
WP_x_n	I	**Write Protect** The Write Protect signal disables Flash array program and erase operations.
Vcc	I	**Power** Vcc is the power supply to the device.
VccQ	I	**I/O Power** VccQ is the power supply for input and/or output signals.
VccQL	I	**I/O Power** VccQL is the power supply for input and/or output signals when NV-LPDDR4 with VccQL (PI-LTT) is enabled.
Vpp	I	**High Voltage Power** Vpp is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance Erase and Program operations (e.g., improved power efficiency).
VREFQ_DNU	I	**Voltage Reference** VREFQ Do Not Use (DNU). External voltage reference optionally used on or older NAND devices but not used starting ONFI 6.0 NAND devices. This signal is a placeholder of the ball location of external VREFQ on the package ball map to prevent the balls from being used inadvertently for other purposes.
Vss	I	**Ground** The Vss signal is the power supply ground.
VSP_x		**Vendor Specific** The function of these signals is defined and specified by the NAND vendor. Devices shall have an internal pull-up or pull-down resistor on these signals to yield ONFI compliant behavior when a signal is not connected by the host. Any VSP signal not used by the NAND vendor shall not be connected internal to the device. The VSP signals shall be treated as NU signals by the user.

Signal Name	Input / Output	Description
VssQ	I	**I/O Ground** The VssQ signal is the ground for input and/or output signals.
ZQ_x	na	**Reference pin for ZQ calibration** This is used on ZQ calibration and ZQ signal shall be connected to Vss through RZQ resistor

Table 2-2 SCA Protocol Signal Descriptions

Table 2-3 thru Table 2-6 provide the signal mapping to pin/pad/ball for each package type listed within the ONFI specification. These signal mappings are required if the packages listed in this specification are implemented. If a signal is marked as “na” then the corresponding package does not implement that signal. Any signal that does not have an associated number is implicitly numbered “0”. For example, WP_n is equivalent to WP0_n.

Signal Name	M/O/R	BGA-132 NV-LPDDR4 x8	BGA-152 NV-LPDDR4 x8
R/B0_0_n	M	J4	J5
R/B0_1_n	O	J8	J9
R/B1_0_n	O	J5	J6
R/B1_1_n	O	J7	J8
RE_0_t (n)	M	N5	N6
RE_1_t (n)	O	E7	E8
RE_0_c	M	M7	M8
RE_1_c	O	F5	F6
CE0_0_n	M	K4	K5
CE0_1_n	O	H8	H9
CE1_0_n	O	K5	K6
CE1_1_n	O	H7	H8
CE2_0_n	O	H2	H3
CE2_1_n	O	K10	K11
CE3_0_n	O	H3	H4
CE3_1_n	O	K9	K10
Vcc	M	D7	D8
		J3	J4
		J9	J10
		P5	P6
VccQ	M	D2	D3
		D3	D4
		D9	D10
		D10	D11
		G3	G4
		G9	G10
		L3	L4
		L9	L10
		P2	P3
		P3	P4
		P9	P10
		P10	P11
Vss	M	D5	D6
		J2	J3
		J10	J11
		P7	P8

Signal Name	M/O/R	BGA-132 NV-LPDDR4 x8	BGA-152 NV-LPDDR4 x8
VssQ	M	E2	E3
		E4	E5
		E8	E9
		E10	E11
		G2	G3
		G10	G11
		L2	L3
		L10	L11
		N2	N3
		N4	N5
		N8	N9
		N10	N11
	O	G8	G9
	O	L4	L5
VREFQ_DNU	R	M4	M5
VREFQ_DNU	R	F8	F9
Vpp	O	K7	K8
CLE_0	M	L7	L8
CLE_1	O	G5	G6
ALE_0	M	L8	L9
ALE_1	O	G4	G5
WE_0_n	M	M5	M6
WE_1_n	O	F7	F8
WP_0_n	M	K8	K9
WP_1_n	O	H4	H5
IO0_0 / DQ0_0	M	M10	M11
IO1_0 / DQ1_0	M	M9	M10
IO2_0 / DQ2_0	M	N9	N10
IO3_0 / DQ3_0	M	P8	P9
IO4_0 / DQ4_0	M	P4	P5
IO5_0 / DQ5_0	M	N3	N4
IO6_0 / DQ6_0	M	M3	M4
IO7_0 / DQ7_0	M	M2	M3
IO0_1 / DQ0_1	O	F2	F3
IO1_1 / DQ1_1	O	F3	F4
IO2_1 / DQ2_1	O	E3	E4
IO3_1 / DQ3_1	O	D4	D5
IO4_1 / DQ4_1	O	D8	D9
IO5_1 / DQ5_1	O	E9	E10
IO6_1 / DQ6_1	O	F9	F10
IO7_1 / DQ7_1	O	F10	F11
DQS_0_t	M	N7	N8
DQS_1_t	O	E5	E6

Signal Name	M/O/R	BGA-132 NV-LPDDR4 x8	BGA-152 NV-LPDDR4 x8
DQS_0_c	M	M8	M9
DQS_1_c	O	F4	F5
ZQ_0	M	K3	K4
ZQ_1	O	H9	H10
DBI_0	O	L5	L6
DBI_1	O	G7	G8
SCA_0	M	H10	H11
SCA_1	M	K2	K3

Table 2-3 Signal mappings: BGA-132, and BGA-152 package

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
R/B0_0_n	O	H13	H12
R/B0_1_n	O	R4	R3
R/B0_2_n	O	J13	J12
R/B0_3_n	O	P4	P3
R/B1_0_n	O	H14	H13
R/B1_1_n	O	R3	R2
R/B1_2_n	O	J14	J13
R/B1_3_n	O	P3	P2
RE_0_t (n)	M	K6	K5
RE_1_t (n)	O	N11	N10
RE_2_t (n)	O	L6	L5
RE_3_t (n)	O	M11	M10
RE_0_c	M	K7	K6
RE_1_c	O	N10	N9
RE_2_c	O	L7	L6
RE_3_c	O	M10	M9

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
CE0_0_n	M	K11	K10
CE0_1_n	O	N6	N5
CE0_2_n	O	K10	K9
CE0_3_n	O	N7	N6
CE1_0_n	O	H11	H10
CE1_1_n	O	R6	R5
CE1_2_n	O	J11	J10
CE1_3_n	O	P6	P5
CE2_0_n	O	K13	K12
CE2_1_n	O	N4	N3
CE2_2_n	O	K12	K11
CE2_3_n	O	N5	N4
CE3_0_n	O	H12	H11
CE3_1_n	O	R5	R4
CE3_2_n	O	J12	J11
CE3_3_n	O	P5	P4
Vcc	M	B10	B9
		C14	C13
		D2	D1
		D15	D14
		E2	E1
		K2	K1
		N15	N14
		V15	V14
		W2	W1
		W15	W14
		Y3	Y2
		AA7	AA6
VCCQ	M	B13	B12
	M	C3	C2
	M	G10	G9
	M	G15	G14
	M	H2	H1
	M	R15	R14
	M	T2	T1
	M	T7	T6
	M	Y14	Y13
	M	AA4	AA3

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
VCCQ or VCCQL	M	B4	B3
	M	B11	B10
	M	F15	F14
	M	G2	G1
	M	T15	T14
	M	U2	U1
	M	AA6	AA5
	M	AA13	AA12
VSP2 or R or VCCQL	O	H6	H5
VSP3 or R or VCCQL	O	R11	R10

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
Vss	M	B5	B4
		B6	B5
		B7	B6
		B12	B11
		C4	C3
		C5	C4
		C10	C9
		C11	C10
		C12	C11
		C13	C12
		D3	D2
		D4	D3
		D5	D4
		D12	D11
		D13	D12
		D14	D13
		E3	E2
		E4	E3
		E5	E4
		E12	E11
		E13	E12
		E14	E13
		E15	E14
		F2	F1
		F3	F2
		F4	F3
		F12	F11
		F13	F12
		F14	F13
		G3	G2
		G4	G3
		H3	H2
		H4	H3
		H7	H6
		H15	H14
		J4	J3
		J5	J4
		L12	L11

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
Vss	M	L13	L12
		L14	L13
		L15	L14
		M2	M1
		M3	M2
		M4	M3
		M5	M4
		P12	P11
		P13	P12
		R2	R1
		R10	R9
		R13	R12
		R14	R13
		T13	T12
		T14	T13
		U3	U2
		U4	U3
		U5	U4
		U13	U12
		U14	U13
		U15	U14
		V2	V1
		V3	V2
		V4	V3
		V5	V4
		V12	V11
		V13	V12
		V14	V13
		W3	W2
		W4	W3
		W5	W4
		W12	W11
		W13	W12
		W14	W13
		Y4	Y3
		Y5	Y4
		Y6	Y5
		Y7	Y6
		Y12	Y11
		Y13	Y12
		AA5	AA4
		AA10	AA9
		AA11	AA10
		AA12	AA11

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
VREFQ_DNU	R	L10 L11 M6 M7	L9 L10 M5 M6
Vpp	O	K15 N2	K14 N1
CLE_0	M	K5	K4
CLE_1	O	N12	N11
CLE_2	O	L5	L4
CLE_3	O	M12	M11
ALE_0	M	K4	K3
ALE_1	O	N13	N12
ALE_2	O	L4	L3
ALE_3	O	M13	M12
WE_0_n	M	H10	H9
WE_1_n	O	R7	R6
WE_2_n	O	J10	J9
WE_3_n	O	P7	P6
WP_0_n	M	K3	K2
WP_1_n	O	N14	N13
WP_2_n	O	L3	L2
WP_3_n	O	M14	M13
IO0_0 / DQ0_0	M	C7	C6
IO1_0 / DQ1_0	M	D7	D6
IO2_0 / DQ2_0	M	E7	E6
IO3_0 / DQ3_0	M	F5	F4
IO4_0 / DQ4_0	M	D11	D10
IO5_0 / DQ5_0	M	E11	E10
IO6_0 / DQ6_0	M	F11	F10
IO7_0 / DQ7_0	M	G12	G11
IO0_1 / DQ0_1	O	Y10	Y9
IO1_1 / DQ1_1	O	W10	W9
IO2_1 / DQ2_1	O	V10	V9
IO3_1 / DQ3_1	O	U12	U11
IO4_1 / DQ4_1	O	W6	W5
IO5_1 / DQ5_1	O	V6	V5
IO6_1 / DQ6_1	O	U6	U5
IO7_1 / DQ7_1	O	T5	T4

Signal Name	M/O/R	BGA-272 NV-LPDDR4 x8	BGA-252 NV-LPDDR4 x8
IO0_2 / DQ0_2	O	C6	C5
IO1_2 / DQ1_2	O	D6	D5
IO2_2 / DQ2_2	O	E6	E5
IO3_2 / DQ3_2	O	G5	G4
IO4_2 / DQ4_2	O	D10	D9
IO5_2 / DQ5_2	O	E10	E9
IO6_2 / DQ6_2	O	F10	F9
IO7_2 / DQ7_2	O	G11	G10
IO0_3 / DQ0_3	O	Y11	Y10
IO1_3 / DQ1_3	O	W11	W10
IO2_3 / DQ2_3	O	V11	V10
IO3_3 / DQ3_3	O	T12	T11
IO4_3 / DQ4_3	O	W7	W6
IO5_3 / DQ5_3	O	V7	V6
IO6_3 / DQ6_3	O	U7	U6
IO7_3 / DQ7_3	O	T6	T5
DQS_0_t	M	F7	F6
DQS_1_t	O	U10	U9
DQS_2_t	O	F6	F5
DQS_3_t	O	U11	U10
DQS_0_c	M	G7	G6
DQS_1_c	O	T10	T9
DQS_2_c	O	G6	G5
DQS_3_c	O	T11	T10
VSP0 (R)	O	H5	H4
VSP1 (R)	O	R12	R11
VSP4 (R)	O	K14	K13
VSP5 (R)	O	N3	N2
VSP6 (R)	O	J15	J14
VSP7 (R)	O	P2	P1
ZQ_0	M	G14	G13
ZQ_1	O	T3	T2
ZQ_2	O	G13	G12
ZQ_3	O	T4	T3
DBI_0	O	J7	J6
DBI_1	O	P10	P9
DBI_2	O	J6	J5
DBI_3	O	P11	P10
SCA_0	M	L2	L1
SCA_1	M	M15	M14

Table 2-4 Signal mappings: BGA-272 and BGA-252 package

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
R/B_0_n	O	F11	F11
R/B_1_n	O	U6	U6
R/B_2_n	O	E11	E11
R/B_3_n	O	V6	V6
RE_0_t (n)	M	K10	K10
RE_1_t (n)	O	N7	N7
RE_2_t (n)	O	K7	K7
RE_3_t (n)	O	N10	N10
RE_0_c	M	J10	J10
RE_1_c	O	P7	P7
RE_2_c	O	J7	J7
RE_3_c	O	P10	P10

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
CE0_0_n	M	K12	K12
CE0_1_n	O	N5	N5
CE0_2_n	O	J12	J12
CE0_3_n	O	P5	P5
CE1_0_n	O	H12	H12
CE1_1_n	O	R5	R5
CE1_2_n	O	G12	G12
CE1_3_n	O	T5	T5
CE2_0_n	O	K13	K13
CE2_1_n	O	N4	N4
CE2_2_n	O	J13	J13
CE2_3_n	O	P4	P4
CE4_0_n	O	na	K14
CE4_1_n	O	na	N3
CE4_2_n	O	na	J14
CE4_3_n	O	na	P3
CE5_0_n	O	na	H14
CE5_1_n	O	na	R3
CE5_2_n	O	na	G14
CE5_3_n	O	na	T3
CE6_0_n	O	na	F13
CE6_1_n	O	na	U4
CE6_2_n	O	na	E13
CE6_3_n	O	na	V4
CE7_0_n	O	na	F14
CE7_1_n	O	na	U3
CE7_2_n	O	na	E14
CE7_3_n	O	na	V3
CE3_0_n or VCCQ	O	H13	H13
CE3_1_n or VCCQ	O	R4	R4
CE3_2_n or VCCQL	O	G13	G13
CE3_3 or VCCQL	O	T4	T4

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
Vcc	M	B9	B9
		B11	B11
		B13	B13
		C4	C4
		D2	D2
		D15	D15
		G4	G4
		G15	G15
		H2	H2
		K15	K15
		N2	N2
		R15	R15
		T2	T2
		T13	T13
		W2	W2
		W15	W15
		Y13	Y13
		AA4	AA4
		AA6	AA6
		AA8	AA8
VCCQ	M	B4	B4
	M	F4	F4
	M	G2	G2
	M	L15	L15
	M	M2	M2
	M	T15	T15
	M	U13	U13
	M	AA13	AA13
VCCQ or VCCQL	M	B6	B6
	M	C10	C10
	M	E2	E2
	M	H4	H4
	M	K2	K2
	M	N15	N15
	M	R13	R13
	M	V15	V15
	M	Y7	Y7
	M	AA11	AA11

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
Vss	M	B5	B5
		B7	B7
		B10	B10
		B12	B12
		C3	C3
		C5	C5
		C11	C11
		D3	D3
		D10	D10
		D11	D11
		D12	D12
		D13	D13
		D14	D14
		E3	E3
		E13	
		E14	
		F2	F2
		F3	F3
		F5	F5
		F13	
		F14	
		F15	F15
		G3	G3
		G5	G5
		G14	
		H3	H3
		H5	H5
		H14	
		J4	J4
		J14	
		J15	J15
		K3	K3
		K4	K4
		K14	
		L14	L14
		M3	M3
		N3	
		N13	N13

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
Vss	M	N14	N14
		P2	P2
		P3	
		P13	P13
		R3	
		R12	R12
		R14	R14
		T3	
		T12	T12
		T14	T14
		U2	U2
		U3	
		U4	
		U12	U12
		U14	U14
		U15	U15
		V3	
		V4	
		V14	V14
		W3	W3
		W4	W4
		W5	W5
		W6	W6
		W7	W7
		W14	W14
		Y6	Y6
		Y12	Y12
		Y14	Y14
		AA5	AA5
		AA7	AA7
		AA10	AA10
		AA12	AA12
VREFQ_DNU	R	B8	B8
		L3	L3
		M14	M14
		AA9	AA9
Vpp	O	C14	C14
		Y3	Y3
CLE_0	M	H10	H10
CLE_1	O	R7	R7
CLE_2	O	H11	H11
CLE_3	O	R6	R6

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
ALE_0	M	K11	K11
ALE_1	O	N6	N6
ALE_2	O	J11	J11
ALE_3	O	P6	P6
WE_0_n	M	L10	L10
WE_1_n	O	M7	M7
WE_2_n	O	L7	L7
WE_3_n	O	M10	M10
WP_0_n	M	G10	G10
WP_1_n	O	T7	T7
WP_2_n	O	G11	G11
WP_3_n	O	T6	T6
IO0_0 / DQ0_0	M	M6	M6
IO1_0 / DQ1_0	M	L6	L6
IO2_0 / DQ2_0	M	K6	K6
IO3_0 / DQ3_0	M	J6	J6
IO4_0 / DQ4_0	M	F7	F7
IO5_0 / DQ5_0	M	E7	E7
IO6_0 / DQ6_0	M	D7	D7
IO7_0 / DQ7_0	M	C7	C7
IO0_1 / DQ0_1	O	L11	L11
IO1_1 / DQ1_1	O	M11	M11
IO2_1 / DQ2_1	O	N11	N11
IO3_1 / DQ3_1	O	P11	P11
IO4_1 / DQ4_1	O	U10	U10
IO5_1 / DQ5_1	O	V10	V10
IO6_1 / DQ6_1	O	W10	W10
IO7_1 / DQ7_1	O	Y10	Y10
IO0_2 / DQ0_2	O	M5	M5
IO1_2 / DQ1_2	O	L5	L5
IO2_2 / DQ2_2	O	K5	K5
IO3_2 / DQ3_2	O	J5	J5
IO4_2 / DQ4_2	O	F6	F6
IO5_2 / DQ5_2	O	E6	E6
IO6_2 / DQ6_2	O	D6	D6
IO7_2 / DQ7_2	O	C6	C6
IO0_3 / DQ0_3	O	L12	L12
IO1_3 / DQ1_3	O	M12	M12
IO2_3 / DQ2_3	O	N12	N12
IO3_3 / DQ3_3	O	P12	P12
IO4_3 / DQ4_3	O	U11	U11
IO5_3 / DQ5_3	O	V11	V11
IO6_3 / DQ6_3	O	W11	W11
IO7_3 / DQ7_3	O	Y11	Y11

Signal Name	M/O/R	BGA-316 NV-LPDDR4 x8 16 CE_n	BGA-316 NV-LPDDR4 x8 32 CE_n
DQS_0_t	M	G7	G7
DQS_1_t	O	T10	T10
DQS_2_t	O	G6	G6
DQS_3_t	O	T11	T11
DQS_0_c	M	H7	H7
DQS_1_c	O	R10	R10
DQS_2_c	O	H6	H6
DQS_3_c	O	R11	R11
VSP (R)	O	D4 D5 E4 E5 J2 J3 L4 L13 M4 M13 P14 P15 V12 V13 W12 W13	D4 D5 E4 E5 J2 J3 L4 L13 M4 M13 P14 P15 V12 V13 W12 W13
ZQ_0	M	F12	F12
ZQ_1	O	U5	U5
ZQ_2	O	E12	E12
ZQ_3	O	V5	V5
DBI_0	O	F10	F10
DBI_1	O	U7	U7
DBI_2	O	E10	E10
DBI_3	O	V7	V7
SCA_0	M	~~R2~~ H15	~~R2~~ H15
SCA_1	M	~~H15~~ R2	~~H15~~ R2

Table 2-5 Signal mappings: BGA-316 packages

Signal Name	M/O/R	BGA-178 NV-LPDDR4 x8	BGA-154 NV-LPDDR4 x8	BGA-146 NV-LPDDR4 x8
R/B0_0_n	M	F8	F7	H8
R/B0_1_n	O	K8	K7	H4
R/B1_0_n	O	G8	G7	H7
R/B1_1_n	O	J8	J7	H5
RE_0_t (n)	M	G4	G3	D7
RE_1_t (n)	O	J12	J11	M5
RE_0_c	M	G5	G4	E7
RE_1_c	O	J11	J10	L5
CE0_0_n	M	E8	E7	H9
CE0_1_n	O	L8	L7	H3
CE1_0_n	O	E7	E6	G9
CE1_1_n	O	L9	L8	J3
CE2_0_n	O	F7	F6	G8
CE2_1_n	O	K9	K8	J4
CE3_0_n or VCCQ	O	G7	G6	G7
CE3_1_n or VCCQ	O	J9	J8	J5
Vcc	M	C8	C7	H11
		D4	D3	D10
		D12	D11	M10
		G3	G2	C7
		J13	J12	N5
		M4	M3	D2
		M12	M11	M2
		N8	N7	H1
VCCQ	M	C4	C3	D11
	M	C10	C9	K11
	M	C12	C11	M11
	M	D3	D2	C10
	M	D13	D12	N10
	M	M3	M2	C2
	M	M13	M12	N2
	M	N4	N3	D1
	M	N6	N5	F1
	M	N12	N11	M1

Signal Name	M/O/R	BGA-178 NV-LPDDR4 x8	BGA-154 NV-LPDDR4 x8	BGA-146 NV-LPDDR4 x8
VCCQ or	M	E5	E4	E9
VCCQL	M	E11	E10	L9
	M	F3	F2	C8
	M	F13	F12	N8
	M	K3	K2	C4
	M	K13	K12	N4
	M	L5	L4	E3
	M	L11	L10	L3
Vss	M	C5	C4	E11
		C7	C6	G11
		C9	C8	J11
		C11	C10	L11
		E3	E2	C9
		E13	E12	N9
		F5	F4	E8
		F11	F10	L8
		G13	G12	N7
		J3	J2	C5
		K5	K4	E4
		K11	K10	L4
		L3	L2	C3
		L13	L12	N3
		N5	N4	E1
		N7	N6	G1
		N9	N8	J1
		N11	N10	L1
VREFQ_DNU	R	D8	D7	H10
VREFQ_DNU	R	M8	M7	H2
Vpp	O	C6	C5	F11
		D6	D5	F10
		M10	M9	K2
		N10	N9	K1
CLE_0	M	J7	J6	G5
CLE_1	O	G9	G8	J7
ALE_0	M	K7	K6	G4
ALE_1	O	F9	F8	J8
WE_0_n	M	G6	G5	F7
WE_1_n	O	J10	J9	K5
WP_0_n	M	L7	L6	G3
WP_1_n	O	E9	E8	J9

Signal Name	M/O/R	BGA-178 NV-LPDDR4 x8	BGA-154 NV-LPDDR4 x8	BGA-146 NV-LPDDR4 x8
IO0_0 / DQ0_0	M	L6	L5	F3
IO1_0 / DQ1_0	M	K6	K5	F4
IO2_0 / DQ2_0	M	L4	L3	D3
IO3_0 / DQ3_0	M	K4	K3	D4
IO4_0 / DQ4_0	M	F4	F3	D8
IO5_0 / DQ5_0	M	E4	E3	D9
IO6_0 / DQ6_0	M	F6	F5	F8
IO7_0 / DQ7_0	M	E6	E5	F9
IO0_1 / DQ0_1	O	E10	E9	K9
IO1_1 / DQ1_1	O	F10	F9	K8
IO2_1 / DQ2_1	O	E12	E11	M9
IO3_1 / DQ3_1	O	F12	F11	M8
IO4_1 / DQ4_1	O	K12	K11	M4
IO5_1 / DQ5_1	O	L12	L11	M3
IO6_1 / DQ6_1	O	K10	K9	K4
IO7_1 / DQ7_1	O	L10	L9	K3
DQS_0_t	M	J4	J3	D5
DQS_1_t	O	G12	G11	M7
DQS_0_c	M	J5	J4	E5
DQS_1_c	O	G11	G10	L7
VSP0	O	M5	M4	E2
VSP1	O	D11	D10	L10
VSP2	O	M6	M5	F2
VSP3	O	D10	D9	K10
ZQ_0	M	D7	D6	G10
ZQ_1	O	M9	M8	J2
DBI_0	O	J6	J5	F5
DBI_1	O	G10	G9	K7
SCA_0	M	M7	M6	G2
SCA_1	M	D9	D8	J10

Table 2-6 Signal mappings: BGA-178, BGA-154 and BGA-146 packages

2.5. CE_n / CA_CE_n Signal Requirements

If one or more LUNs are active and the host sets CE_n (Conv. Protocol) / CA_CE_n (SCA Protocol) to one, then those operations continue executing until completion at which point the NAND Target enters standby. After the CE_n / CA_CE_n signal is transitioned to one, the host may drive a different CE_n / CA_CE_n signal to zero and begin operations on another NAND Target. In Conv. Protocol if using a dual x8 package (e.g. BGA-154), then operations may execute in parallel on two different CE_n signals if they are connected to different 8-bit data buses.

When SR[6] for a particular LUN is cleared to zero and the CE_n / CA_CE_n signal for the corresponding NAND Target is pulled low, the host may only issue the Reset, Synchronous Reset, Reset LUN, Read Status, Read Status Enhanced, or Volume Select (Volume Select only applicable for the Conv. Protocol) commands to that LUN.

2.6. Absolute Maximum DC Ratings

Stresses greater than those listed in the table below may cause permanent damage to the device. This is a stress rating only. The table below defines the voltage on any pin relative to Vss and/or VssQ.

Parameter	Symbol	Rating	Units
VPP Supply Voltage	V_{PP}	-0.6 to +16	V
Vcc = 2.5V and VccQ = 1.2V nominal			
Vcc Supply Voltage	V_{CC}	-0.3 to +3.2	V
Voltage Input	V_{IN}	-0.2 to +1.5	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +1.5	
Vcc = 2.5V, VccQ = 1.2V and VccQL = 0.6V nominal			
Vcc Supply Voltage	V_{CC}	-0.3 to +3.2	V
Voltage Input	V_{IN}	-0.2 to +1.5	
VccQ Supply Voltage	V_{CCQ}	-0.2 to +1.5	
VccQL Supply Voltage	V_{CCQL}	-0.2 to +1.5	

Table 2-7 Absolute maximum DC ratings

2.7. Recommended DC Operating Conditions

Operation beyond the recommended operating conditions is not recommended, exposure beyond these conditions may affect device reliability.

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage for 2.5V devices [1,2]	V_{CC}	2.35	2.5	2.75	V
Supply voltage for 1.2V I/O signaling[1,2]	V_{CCQ}	1.14	1.2	1.26	V
Supply voltage for 0.6V I/O (PI-LTT) signaling[1,2,3]	V_{CCQL}	0.57	0.60	0.63	V
Ground voltage supply	V_{SS}	0	0	0	V
Ground voltage supply for I/O signaling	V_{SSQ}	0	0	0	V
External voltage supply	V_{PP}	10.8	12.0	13.2	V

NOTE:
1. AC Noise on the Vcc, VccQ and VccQL supply voltages shall not exceed +/- 3% of Typ voltage.
2. AC and DC noise together at the NAND ball shall stay within the Min-Max range specified in this table.
3. VccQL (PI-LTT) is an optional supply for NAND devices to support. When the NAND device does not support VccQL or the application that uses the NAND device does not support VccQL operation, then the VccQL balls shall be treated as VccQ balls and be supplied with the VccQ recommended supply range specified in this table. When the NAND device supports VccQL and the application supports VccQL, when enabling VccQL mode on the NAND device and operating in VccQL mode, the voltage on the VccQL supply shall be within the VccQL recommended range specified in this table.

Table 2-8 Recommended DC Operating Conditions

Parameter	Symbol	Max Z(f) Freq: 2Mhz to 10Mhz	Max Z(f) Freq: 20Mhz	Units
Power supply impedance for 2.5V supply [1, 2]	Z(f)_V_{CC}	TBD	TBD	mΩ
Power supply impedance for 1.2V I/O supply[1, 2]	Z(f)_V_{CCQ}	10	20	mΩ
Power supply impedance for 0.6V I/O supply[1, 2]	Z(f)_V_{CCQL}	10	20	mΩ
External voltage supply [1, 2]	Z(f)_V_{PP}	TBD	TBD	mΩ

NOTE:
1. Z(f) is defined for all pins per voltage domain.
2. Z(f) does not include the NAND package and silicon die.

Table 2-9 Power Supply Impedance Requirements

2.8. AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from VccQ or VccQL (VccQL for NV-LPDDR4 with VccQL, also known as PI-LTT) and Vss/VssQ levels. Table 2-10 defines the maximum values that the AC overshoot or undershoot may attain.

The maximum overshoot area above VccQ/VccQL and the maximum undershoot area below Vss/VssQ is symmetric and varies depending on timing mode; refer to Table 2-10. These values apply to the maximum data signaling frequency for a given timing mode. If the data signaling frequency for maximum overshoot or undershoot conditions is less than the selected timing mode, then the values for the applicable slower timing mode may be used.

NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the controller. If the controller has more stringent requirements termination or other means of reducing overshoot or undershoot may be required to reduce beyond the NAND requirements.

Parameter	Maximum Overshoot above VccQ and Maximum Undershoot below VssQ	
	Area	Amplitude
	I/O signals and RE_t/RE_c	All signals
Timing Mode 0-1	2.00 V-ns	0.30 V
Timing Mode 2	1.20 V-ns	
Timing Mode 3	0.96 V-ns	
Timing Mode 4	0.80 V-ns	
Timing Mode 5	0.60 V-ns	
Timing Mode 6	0.48 V-ns	
Timing Mode 7	0.40 V-ns	
Timing Mode 8	0.30 V-ns	
Timing Mode 9	0.24 V-ns	
Timing Mode 10	0.20 V-ns	
Timing Mode 11	0.15 V-ns	
Timing Mode 12	0.13 V-ns	
Timing Mode 13	0.12 V-ns	
Timing Mode 14	0.11 V-ns	
Timing Mode 15	0.10 V-ns	
Timing Mode 16	0.09 V-ns	
Timing Mode 17	0.08 V-ns	
Timing Mode 18	0.073 V-ns	
Timing Mode 19	0.067 V-ns	
Timing Mode 20	0.057 V-ns	
Timing Mode 21	0.050 V-ns	
Timing Mode 22	0.044 V-ns	
Timing Mode 23	0.040 V-ns	
Timing Mode 24	0.038 V-ns	
Timing Mode 25	0.036 V-ns	
Timing Mode 26	0.033 V-ns	
NOTE 1: Intended for devices with no clamp protection and is guaranteed by design.		

Table 2-10 NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) AC Overshoot/Undershoot Maximum Values

The figure below displays pictorially the parameters described in Table 2-10.

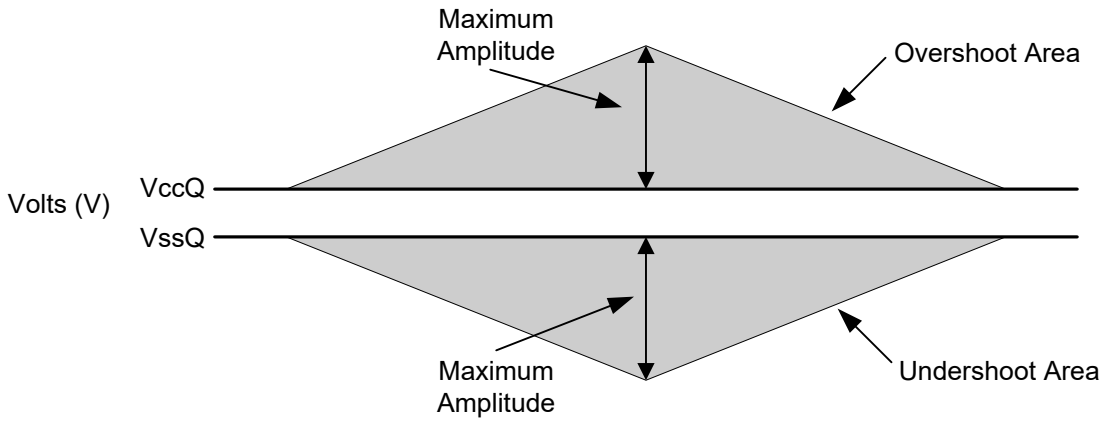


Figure 2-16 AC Overshoot/Undershoot Diagram

2.9. Input AC/DC Levels

2.9.1. Single-Ended Input AC/DC Levels

2.9.1.1. NV-LPDDR4 (LTT)

The following tables show the input level requirements for various signals. For all signals, the receiver will effectively switch as a result of the signal crossing the AC input level and remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC Input high voltage unterminated	VIH.UNTERM.LTT[3,4] (DC)	-	VccQ * 0.5	-	VccQ	mV
AC Input high voltage unterminated	VIH.UNTERM.LTT[3,4] (AC)	-	VccQ *0.5	-	(Note 1)	mV
DC Input low voltage unterminated	VIL.UNTERM.LTT[3,4] (DC)	-	Vss	-	80	mV
DC Input low voltage unterminated	VIL.UNTERM.LTT[3,4] (AC)	-	(Note 1)	-	60	mV
DC Input high voltage	VIH.LTT[3,5] (DC)	Timing mode 0 - 21	Vcent_DQ + 80	-	VccQ	mV
		Timing mode 22 – 26	Vcent_DQ + 60			
AC Input high voltage	VIH.LTT[3,5] (AC)	Timing mode 0 – 21	Vcent_DQ + 100	-	(Note 1)	mV
		Timing mode 22 – 26	Vcent_DQ + 85			
DC Input low voltage	VIL.LTT[3,5] (DC)	Timing mode 0 – 21	VssQ	-	Vcent_DQ - 80	mV
		Timing mode 22 – 26			Vcent_DQ - 60	
AC Input low voltage	VIL.LTT[3,5] (AC)	Timing mode 16 - 21	(Note 1)	-	Vcent_DQ - 100	mV
		Timing mode 22 - 26			Vcent_DQ - 85	
DQ RX Mask Voltage total	VDIVW.LTT[6]	Timing mode 16 - 21	160	-	-	mV
		Timing mode 22 - 26	120			
DQ AC Input pulse amplitude pk-pk	VIHL.LTT [7] (AC)	Timing mode 16 - 21	200	-	-	mV
		Timing mode 22 - 26	170			
DC Input high voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIH.CMOS[2] (DC)	-	VccQ * 0.7	-	VccQ	mV
AC Input high voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIH.CMOS[2] (AC)	-	VccQ *0.8	-	(Note 1)	mV
DC Input low voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIL.CMOS[2] (DC)	-	Vss	-	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIL.CMOS[2] (AC)	-	(Note 1)	-	VccQ * 0.2	mV
NOTES:						

1. Refer to AC Overshoot and Undershoot requirements.
2. CE_n, WE_n, ALE, CLE and WP_n are CMOS signals and do not use LTT levels.
3. These specs apply to RE_t/RE_c, DQS_t/DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t and DQS_c these are single-ended signal requirements.
4. Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled. NAND vendors may support a higher VIL.UNTERM.LTT or lower VIH.UNTERM.LTT specifications. See vendor datasheet.
5. Vcent_DQ shall be regarded as Vcent_RE, Vcent_DQS and Vcent_DQ for RE_t/RE_c, DQS_t/DQS_c, DBI and DQ[7:0] signals respectively.
6. For DQ signals, DQ Rx Mask specifiations are aligned to DC requirements and VIHL.LTT (AC) specification is aligned to AC signal requirements.The signal input pulse amplitude must meet or exceed VIHL.LTT (AC) at any point over the total UI, except when no transitions are occurring for that UI. VIHL.LTT (AC) is centered around Vcent_DQ (pin_mid) such that [VIHL.LTT (AC) (min)] / 2 must be met both above and below Vcent_DQ (pin_mid). There are no timing requirements above or below VIHL.LTT (AC) levels.

Table 2-11 Single-Ended AC/DC Input Levels for NV-LPDDR4 (LTT)

2.9.1.2. NV-LPDDR4 with VccQL (PI-LTT) AC/DC Levels

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC Input high voltage unterminated	VIH.UNTERM.PILTT[3,4] (DC)	-	VccQL * 0.85	-	VccQL	mV
AC Input high voltage unterminated	VIH.UNTERM.PILTT[3,4] (AC)	-	VccQL * 0.90	-	(Note 1)	mV
DC Input low voltage unterminated	VIL.UNTERM.PILTT[3,4] (DC)	-	Vss	-	80	mV
DC Input low voltage unterminated	VIL.UNTERM.PILTT[3,4] (AC)	-	(Note 1)	-	60	mV
DC Input high voltage	VIH.PILTT[3,5] (DC)	Timing mode 0 - 21	Vcent_DQ + 80	-	VccQL	mV
		Timing mode 22 – 26	Vcent_DQ + 60			
AC Input high voltage	VIH.PILTT[3,5] (AC)	Timing mode 0 – 21	Vcent_DQ + 100	-	(Note 1)	mV
		Timing mode 22 – 26	Vcent_DQ + 85			
DC Input low voltage	VIL.PILTT[3,5] (DC)	Timing mode 0 – 21	Vss	-	Vcent_DQ - 80	mV
		Timing mode 22 – 26			Vcent_DQ - 60	
AC Input low voltage	VIL.PILTT[3,5] (AC)	Timing mode 16 - 21	(Note 1)	-	Vcent_DQ - 100	mV
		Timing mode 22 - 26			Vcent_DQ - 85	
DQ RX Mask Voltage total	VDIVW.PILTT[6]	Timing mode 16 - 21	160	-	-	mV
		Timing mode 22 - 26	120			
DQ AC Input pulse amplitude pk-pk	VIHL.PILTT [7] (AC)	Timing mode 16 - 21	200	-	-	mV
		Timing mode 22 - 26	170			
DC Input high voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIH.CMOS[2] (DC)	-	VccQ * 0.7	-	VccQ	mV
AC Input high voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIH.CMOS[2] (AC)	-	VccQ *0.8	-	(Note 1)	mV
DC Input low voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIL.CMOS[2] (DC)	-	Vss	-	VccQ * 0.3	mV
AC Input low voltage (CE_n, WP_n, CLE, ALE, WE_n)	VIL.CMOS[2] (AC)	-	(Note 1)	-	VccQ * 0.2	mV

NOTES:

1. Refer to AC Overshoot and Undershoot requirements.
2. CE_n, WE_n, ALE, CLE and WP_n are CMOS signals and do not use PI-LTT levels.
3. These specs apply to RE_t/RE_c, DQS_t/DQS_c, DQ[7:0] and DBI. For RE_t, RE_n, DQS_t and DQS_c these are single-ended signal requirements.
4. Termination is disabled during command cycles, address cycles and during data input/output cycles when ODT from the NAND (target and non-target) and the controller are disabled. NAND vendors may support a higher VIL.UNTERM.PILTT or lower VIH.UNTERM.PILTT specifications. See vendor datasheet.
5. Vcent_DQ shall be regarded as Vcent_RE, Vcent_DQS and Vcent_DQ for RE_t/RE_c, DQS_t/DQS_c, DBI and DQ[7:0] signals respectively.
6. For DQ signals, DQ Rx Mask specifiations are aligned to DC requirements and VIHL.PILTT (AC) specification is aligned to AC signal requirements.The signal input pulse amplitude must meet or exceed VIHL.PILTT (AC) at

any point over the total UI, except when no transitions are occurring for that UI. VIHL.PILTT (AC) is centered around Vcent_DQ (pin_mid) such that [VIHL.PILTT (AC) (min)] / 2 must be met both above and below Vcent_DQ (pin_mid). There are no timing requirements above or below VIHL.PILTT (AC) levels.

Table 2-12 Single-Ended AC/DC Input Levels for NV-LPDDR4 with VccQL (PI-LTT)

2.9.2. Controller DQ Rx Mask Levels

The Controller DQ RX Mask specifications in the table below are applicable to controllers that support the data rates listed in the tables below. These specifications do not apply to NAND component.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DQ RX Mask Voltage total	VDIVW.CTLR	Timing mode 0 - 21	160	-	-	mV
		Timing mode 22	120			
		Timing mode 23 - 26	100			

NOTES:
1. The controller DQ Rx mask specifications in this table apply to both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT)
2. The controller DQ Rx mask specification is only for reference and smaller value might be required depending on system. System designers should use IBIS model to close overall system timings

Table 2-13 Controller DQ RX Mask Conditions

2.9.1. Differential AC/DC Levels

The differential AC and DC input levels are defined in the table below. These levels are used to calculate differential signal slew rate.

Interface	Parameter	Symbol	Min	Max	Units
NV-LPDDR4 (LTT)	Differential input high DC	VIHdiff.LTT (DC)	2 x [VIH.LTT (DC) – Vcent]	Refer to Note 1.	V
	Differential input low DC	VILdiff.LTT (DC)	Refer to Note 1.	2 x [VIL.LTT (DC) – Vcent]	V
	Differential input high AC	VIHdiff.LTT (AC)	2 x [VIH.LTT (AC) – Vcent]	Refer to Note 1.	V
	Differential input low AC	VILdiff.LTT (AC)	Refer to Note 1.	2 x [VIL.LTT (AC) – Vcent]	V
NV-LPDDR4 with VccQL (PI-LTT)	Differential input high DC	VIHdiff.PILTT (DC)	2 x [VIH.PILTT (DC) – Vcent]	Refer to Note 2.	V
	Differential input low DC	VILdiff.PILTT (DC)	Refer to Note 2.	2 x [VIL.PILTT (DC) – Vcent]	V
	Differential input high AC	VIHdiff.PILTT (AC)	2 x [VIH.PILTT (AC) – Vcent]	Refer to Note 2.	V
	Differential input low AC	VILdiff.PILTT (AC)	Refer to Note 2.	2 x [VIL.PILTT (AC) – Vcent]	V

NOTE:
1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH.LTT(DC) max, VIL.LTT (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot as specified in the AC Overshoot/Undershoot Requirements section.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [VIH.PILTT(DC) max, VIL.PILTT (DC) min] for single-ended signals as well as the limitations for overshoot and undershoot as specified in the AC Overshoot/Undershoot Requirements section.

Table 2-14 Differential AC and DC Input Levels

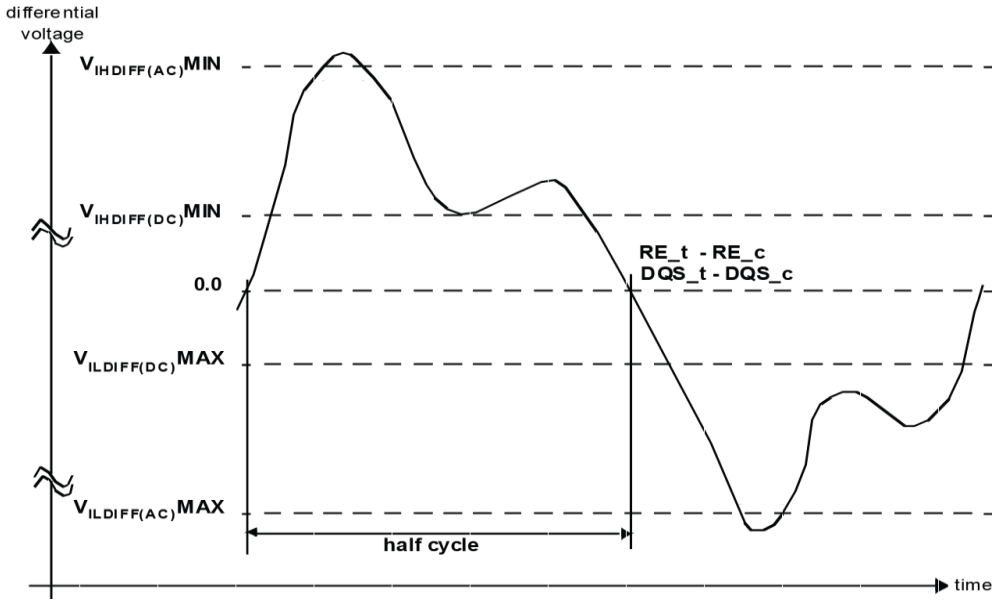


Figure 2-17 Definition of Differential AC Swing

Parameter	Symbol	Up to 3200 MT/s	>3200 MT/s up to 4800 MT/s	Unit
AC differential input cross-point voltage	$V_{IX.LTT.TERM}$	VREFDQ ± 0.064	VREFDQ ± 0.054	V

NOTES:
1. For NV-LPDDR4 (LTT), the typical value of VIX is expected to be about VREFDQ of the NAND Flash Memory internal setting value by VREF Training and VIX is expected to track variations in VREFDQ. VIX indicates the voltage at which differential input signals must cross.
2. VIX value for unterminated condition is VSP

Table 2-15 Differential Vix Levels for NV-LPDDR4 (LTT)

Parameter	Symbol	Up to 3200 MT/s	>3200 MT/s up to 4800 MT/s	Unit
AC differential input cross-point voltage	$V_{IX.PI-LTT.TERM}$	VREFDQ ± 0.064	VREFDQ ± 0.054	V

NOTES:
3. For NV-LPDDR4 with VccQL (PI-LTT), the typical value of VIX is expected to be about VREFDQ of the NAND Flash Memory internal setting value by VREF Training and VIX is expected to track variations in VREFDQ. VIX indicates the voltage at which differential input signals must cross.
4. VIX value for unterminated condition is VSP

Table 2-16 Differential Vix Levels for NV-LPDDR4 with VccQL (PI-LTT)

2.9.2. Internal VREFQ Specifications

The tables below show the minimum required range of NAND internal VREFQ. NAND devices may offer a wider allowable range (see vendor datasheet). A host shall not set the NAND internal VREFQ to a setting beyond the allowable range even during Write Training Internal VREFQ training. These specs define the allowable range for NAND internal VrefQ settings but does not represent the needed settings for high-speed operations. The needed setting for high-speed operations is obtained from either NAND vendor recommendation or through Internal VrefQ Training. NAND Devices could support either Value1 or Value3 settings (see vendor datasheet)

Interface	Parameter	Symbol	Min	Max	Unit
NV-LPDDR4 (LTT)	Minimum allowable range upper limit	VREFQ1.HI.LTT	-	0.40 x VccQ	V
	Minimum allowable range lower limit	VREFQ1.LO.LTT	160	-	mV
	Internal VREFQ Tolerance	VREFQ1.TOL.LTT	-1.75%	+1.75%	VccQ
NV-LPDDR4 with VccQL (PI-LTT)	Minimum allowable range upper limit	VREFQ1.HI.PILTT	-	0.60 x VccQL	V
	Minimum allowable range lower limit	VREFQ1.LO.PILTT	80	-	mV
	Internal VREFQ Tolerance	VREFQ1.TOL.PILTT	-2.63%	+2.63%	VccQL

Table 2-17 Internal VREFQ specifications for Value1

Interface	Parameter	Symbol	Min	Max	Unit
NV-LPDDR4 (LTT)	Minimum allowable range upper limit	VREFQ3.HI.LTT	-	0.3175 x VccQ	V
	Minimum allowable range lower limit	VREFQ3.LO.LTT	160	-	mV
	Internal VREFQ Tolerance	VREFQ3.TOL.LTT	-1.75%	+1.75%	VccQ
NV-LPDDR4 with VccQL (PI-LTT)	Minimum allowable range upper limit	VREFQ3.HI.PILTT	-	0.50 x VccQL	V
	Minimum allowable range lower limit	VREFQ3.LO.PILTT	80	-	mV
	Internal VREFQ Tolerance	VREFQ3.TOL.PILTT	-2.63%	+2.63%	VccQL

Table 2-18 Internal VREFQ specifications for Value3

2.9.3. Input Waveform Monotonicity Requirement

NAND input circuitry becomes more susceptible to input waveform monotonicity as interface data rate goes up. The input waveform of differential DQS_t/DQS_c, differential RE_t/RE_c and WE_n_x (CA_CLK_x) shall be monotonic in slope between Pt-A and Pt-B in the diagram below:

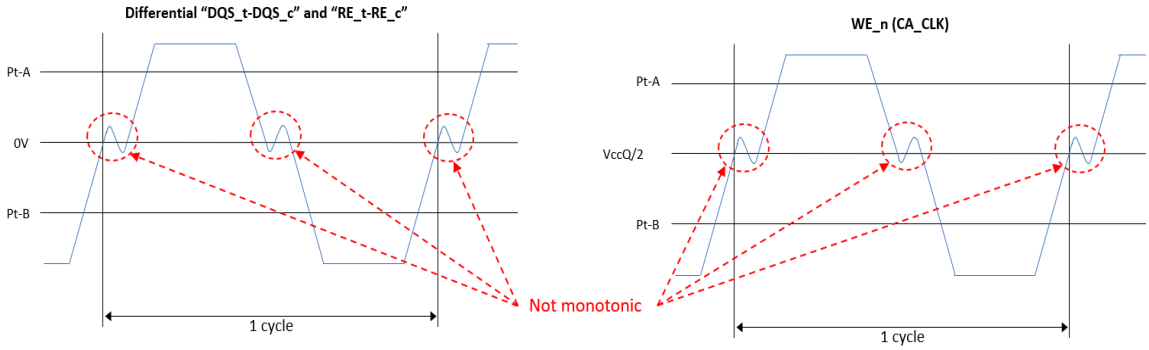


Figure 2-18 Input Waveform Pt-A and Pt-B Diagram

Input Signal	NV-LPDDR (LTT)		NV-LPDDR4 with VccQL (PI-LTT)	
	Pt-A	Pt-B	Pt-A	Pt-B
Differential DQS (DQS_t – DQS_c)	VIH.LTT(DC)(Min) – VIL.LTT(DC)(Max)	VIL.LTT(DC)(Max) – VIH.LTT(DC)(Min)	VIH.PILTT(DC)(Min) – VIL.PILTT(DC)(Max)	VIL.PILTT(DC)(Max) – VIH.PILTT(DC)(Min)
Differential RE (RE_t – RE_c)	VIH.LTT(DC)(Min) – VIL.LTT(DC)(Max)	VIL.LTT(DC)(Max) – VIH.LTT(DC)(Min)	VIH.PILTT(DC)(Min) – VIL.PILTT(DC)(Max)	VIL.PILTT(DC)(Max) – VIH.PILTT(DC)(Min)
Single-Ended WE_n (CA_CLK)	VIH.CMOS(DC)(Min)	VIL.CMOS(DC)(Max)	VIH.CMOS(DC)(Min)	VIL.CMOS(DC)(Max)

Table 2-19 Input Waveform Monoticity Pt-A and Pt-B Definition

The range to keep monotonic slope in unterminated condition for differential DQS and RE is vendor specific.

2.10. Power/Current Specifications

All operating current ratings in this section are specified per active logical unit (LUN). A LUN is active when there is a command outstanding to it. All other current ratings in this section are specified per LUN (regardless of whether it is active).

The test conditions and measurement methodology for the ICC values is defined in the Appendix.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Array read current	ICC1	Refer to Appendix	-	-	100/150/200/235[6]	mA
Array program current	ICC2		-	-	100/150/200/235[6]	mA
Array erase current	ICC3		-	-	100	mA
I/O burst read current	ICC4R		-	-	50/100/135/180/250/300[4]	mA
	ICCQ4R[3]		-	-	50/100/135/180/250/300[4]	mA
I/O burst write current	ICC4W		-	-	50/100/135/180/250/300[4]	mA
	ICCQ4W[3]		-	-	50/100/135/180/250/300[4]	mA
Bus idle current	ICC5		-	-	15	mA
	ICCQ5		-	-	15	mA
Standby current	ISB	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	100/200/270[7]	µA
	ISBQ[8]	CE_n=VccQ-0.2V, WP_n=0V/VccQ	-	-	125	µA
Staggered power-up current from Vcc supply	IST	CE_n=VccQ-0.2V tRise = 1 ms cLine = 0.1 µF	-	-	10	mA
Vpp Idle current	IPPI[5]	-	-	-	10	uA
Vpp Active current	IPPA[5]	-	-	-	15	mA
Input leakage current	ILI[9]	VIN=0V to VccQ (LTT), VIN to VccQL (PI-LTT)	-	-	±10	µA
Output low current (R/B_n)	IOL(R/B_n)	VOL=0.2 V	3	4	-	mA

NOTE:

1. ICC1, ICC2, and ICC3 as listed in this table are active current values. For details on how to calculate the active current from the measured values, refer to Appendix.
2. During cache operations, increased ICC current is allowed while data is being transferred on the bus and an array operation is ongoing. For a cached read this value is ICC1 + $ICC4_R$; for a cached write this value is ICC2(active) + $ICC4_W$.
3. For $ICCQ4_R$ and $ICCQ4_W$ the test conditions in Appendix specify IOUT = 0 mA. When Iout is not equal to 0 mA, additional VccQ switching current will be drawn that is highly dependent on system configuration. IccQ due to loading without IOUT = 0 mA may be calculated for each output pin assuming 50% data switching as (IccQ = 0.5 * C_L * VccQ * frequency), where C_L is the capacitive load.
4. When the data frequency is above 3600MT/s and below or equal to 4800MT/s, then the LUN may consume up to 300 mA. When the data frequency is above 2400 MT/s and below or equal to 3600MT/s, then the LUN may consume up to 250 mA. When the data frequency is above 800 MT/s and below or equal to 2400MT/s, then the LUN may consume up to 180 mA. When the data frequency is above 400MT/s and below or equal to 800 MT/s, then the LUN may consume up to 135 mA. When the data frequency is above 200 MT/s and below or equal to 400 MT/s, then the LUN may consume up to 100 mA. When the data frequency is below or equal to 200 MT/s, then the LUN may consume up to 50 mA.
5. IPP Idle current is IPP current measured when Vpp is supplied and Vpp is not enabled via Set Feature. IPP Active current is IPP current measured when Vpp is supplied and Vpp is enabled via Set Feature.
6. When the data frequency is above 3600MT/s and below or equal to 4800MT/s, then the LUN may consume up to 235 mA. When the data frequency is above 2400 MT/s and below or equal to 3600MT/s, then the LUN may consume up to 200 mA. When the data frequency is above 1600 MT/s and below or equal to 2400MT/s, then the LUN may consume up to 150 mA. When the data frequency is below or equal to 1600 MT/s, then the LUN may consume up to 100 mA.
7. For LUNs that support a maximum data frequency above 3600MT/s and below or equal to 4800MT/s, the ISB Max limit is 270 µA. For LUNs that support a maximum data frequency above 2400 MT/s and below or equal to 3600MT/s, the ISB Max limit is 200 µA. For LUNs that support a maximum data frequency below or equal to 2400 MT/s, the ISB Max limit is 100 µA.
8. During ISBQ testing, DQS_t/DQS_c, RE_t/RE_c, DQ[7:0] and DBI are floating.
9. ILI is tested across the entire recommended VccQ (LTT) or VccQL (PI-LTT) range.

Table 2-20 Current Specifications for Raw NAND on Vcc, VccQ, VccQL or Vpp

The table below specifies the output leakage current requirements (ILO) across the entire allowed VccQ/VccQL ranges specified in Table 2-8.

Symbol	Parameter	Max
ILO_{pd}	Output leakage current: DQ are disabled, VOUT=VccQ for NV-LPDDR4 (LTT) or VOUT=VccQL for NV-LPDDR4 with VccQL (PI-LTT)	20uA[1]
ILO_{pu}	Output leakage current: DQ are disabled, ODT disabled, VOUT=0V for both NV-LPDDR4 (LTT) and NV-LDDR4 with VccQL (PI-LTT)	20uA[1]
NOTE: 1. Absolute leakage value per DQ pin per NAND die. The following signals are required to meet output leakage (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c)		

Table 2-21 Output Leakage

2.10.1. Staggered Power-up

Subsystems that support multiple Flash devices may experience power system design issues related to the current load presented during the power-on condition. To limit the current load presented to the host at power-on, all devices shall support power-up in a low-power condition.

Until a Reset (FFh) command is received by the NAND Target after power-on, the NAND Target shall not draw more than IST of current per LUN from the Vcc supply. For example, a NAND Target that contains 4 LUNs may draw up to 40 mA of current until a Reset (FFh) command is received after power-on.

This value is measured with a nominal rise time (tRise) of 1 millisecond and a line capacitance (cLine) of 0.1 µF. The measurement shall be taken with 1 millisecond averaging intervals and shall begin after the following:

- For NV-LPDDR4 (LTT), when Vcc reaches Vcc_min and VccQ reaches VccQ_min.
- For NV-LPDDR4 with VccQL (PI-LTT), when Vcc reaches Vcc_min and VccQ reaches VccQ_min and VccQL reaches VccQL_min

2.11. Power Cycle Requirements

For the NV-LPDDR4 (LTT) interface, as part of a power cycle, the host shall hold both Vcc and VccQ voltages levels below 100 mV for a minimum time of 100 ns.

For the NV-LPDDR4 with VccQL (PI-LTT) interface, as part of a power cycle, the host shall hold Vcc, VccQ and VccQL voltage levels below 100 mV for a minimum time of 100 ns.

If these requirements are not met as part of a power cycle operation, the device may enter an indeterminate state.

2.12. Independent Data Buses

There may be two independent 8-bit data buses on some ONFI packages (i.e., the BGA-132 and BGA-154 packages). There may be four independent 8-bit data buses in some ONFI packages (i.e. the BGA-316 and BGA-272 packages).

Some signals have a channel (i.e. 8-bit data bus) designator in their name: for example, “x” in CE0_x_n. A signal that has a designator for a certain channel cannot be used for another channel. For example, CE0_0_n cannot be used for any channel other than channel 0 or R/B0_1_n cannot be used for any channel other than channel 1.

In some package configurations, there are multiple CE_n signals per R/B_n signal. Table 2-22 describes the R/B_n signal that each CE_n uses in the case when there are two R/B_n signals and more than one CE_n per 8-bit data bus. Table 2-23 describes the R/B_n signal that each CE_n uses in the case when there is a single R/B_n signal per 8-bit data bus. Table 2-24 provides the case when there is a single CE_n and two R/B_n signals per 8-bit data bus. For packages that only support two 8-bit data buses, R/B0_2_n, R/B1_2_n, R/B0_3_n and R/B1_3_n shall be ignored.

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE2_0_n, CE4_0_n, CE6_0_n
R/B0_1_n	CE0_1_n, CE2_1_n, CE4_1_n, CE6_1_n
R/B0_2_n	CE0_2_n, CE2_2_n, CE4_2_n, CE6_2_n
R/B0_3_n	CE0_3_n, CE2_3_n, CE4_3_n, CE6_3_n
R/B1_0_n	CE1_0_n, CE3_0_n, CE5_0_n, CE7_0_n
R/B1_1_n	CE1_1_n, CE3_1_n, CE5_1_n, CE7_1_n
R/B1_2_n	CE1_2_n, CE3_2_n, CE5_2_n, CE7_2_n
R/B1_3_n	CE1_3_n, CE3_3_n, CE5_3_n, CE7_3_n

Table 2-22 R/B_n Signal Use per CE_n with two R/B_n signals per channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n, CE1_0_n, CE2_0_n, CE3_0_n, CE4_0_n, CE5_0_n, CE6_0_n, CE7_0_n
R/B0_1_n	CE0_1_n, CE1_1_n, CE2_1_n, CE3_1_n, CE4_1_n, CE5_1_n, CE6_1_n, CE7_1_n
R/B0_2_n	CE0_2_n, CE1_2_n, CE2_2_n, CE3_2_n, CE4_2_n, CE5_2_n, CE6_2_n, CE7_2_n
R/B0_3_n	CE0_3_n, CE1_3_n, CE2_3_n, CE3_3_n, CE4_3_n, CE5_3_n, CE6_3_n, CE7_3_n

Table 2-23 R/B_n Signal Use per CE_n with a single R/B_n signal per channel

Signal Name	CE_n
R/B0_0_n	CE0_0_n
R/B0_1_n	CE0_1_n
R/B0_2_n	CE0_2_n
R/B0_3_n	CE0_3_n
R/B1_0_n	CE1_0_n
R/B1_1_n	CE1_1_n
R/B1_2_n	CE1_2_n
R/B1_3_n	CE1_3_n

Table 2-24 R/B_n Signal Use per CE_n with a two R/B_n signals per channel and one CE_n per channel

Implementations may tie the data lines and control signals (RE_n, CLE, ALE, WE_n, WP_n, and DQS) together for the two independent 8-bit data buses externally to the device.

2.13. Power Sequence and Ready/Busy (R/B_n) Requirements

2.13.1. Power Sequence Requirements

During power-on, VccQ and VccQL (if applicable) shall be less than or equal to Vcc at all times. The figure below shows VccQ and VccQL (if applicable) ramping after Vcc, however, they may ramp at the same time.

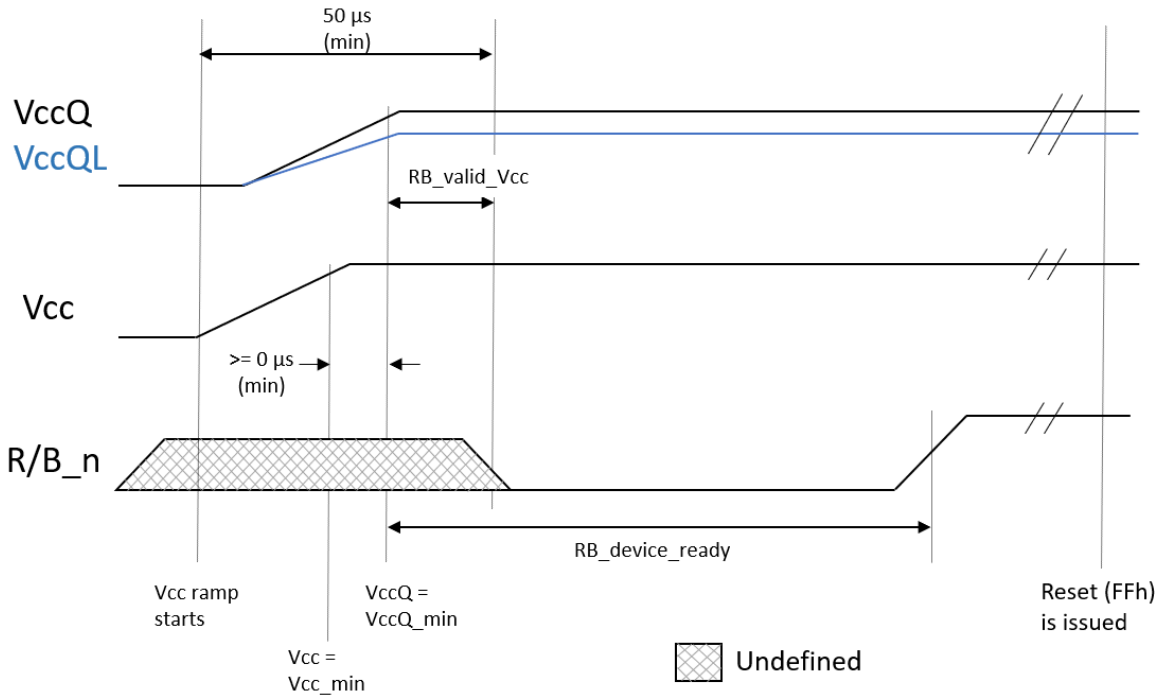


Figure 2-19 Power-On Sequence and R/B_n Power-On Behavior

When users boot up or power down a NAND device, VccQ must be equal or higher than VccQL. NAND devices only allow the four cases power-on/power-off as shown in the following figure :

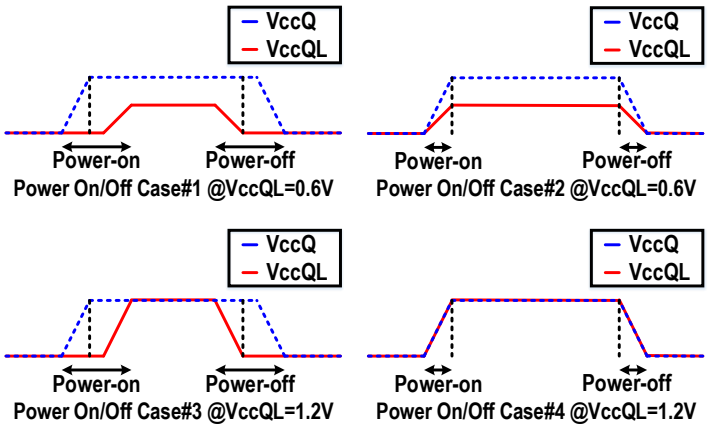


Figure 2-20 VccQ and VccQL Power-On/Off when Boot-Up or Power-Down

Once V_{CC} , VccQ and VccQL (if applicable) reach the V_{CC} minimum, VccQ minimum and VccQL minimum values, respectively, listed in Table 2-8 and power is stable, the R/B_n signal shall be valid after RB_valid_Vcc and shall be set to one (Ready) within RB_device_ready, as listed in Table 2-25. R/B_n is undefined until 50 µs has elapsed after V_{CC} has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

Parameter	NAND
RB_valid_Vcc	10 µs
RB_device_ready	1 ms

Table 2-25 R/B_n Power-on Requirements

Ready/Busy is implemented as an open drain circuit, thus a pull-up resistor shall be used for termination. The combination of the pull-up resistor and the capacitive loading of the R/B_n circuit determines the rise time of R/B_n.

2.13.2. R/B_n and SR[6] Relationship

R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs on the corresponding NAND Target or Volume. In the case that more than one NAND target or Volume share an R/B_n signal, R/B_n shall reflect the logical AND of the SR[6] (Status Register bit 6) values for all LUNs connected to the shared R/B_n signal. For example, R/B0_0 is logical AND of the SR[6] values for all LUNs that share R/B0_0. Thus, R/B_n reflects whether any LUN is busy on a particular NAND Target or if there are multiple NAND Targets that share R/B_n, R/B_n reflects whether any LUN is busy on any of the shared NAND Targets.

2.14. Write Protect

When cleared to zero, the WP_n signal disables Flash array program and erase operations. This signal shall only be transitioned while there are no commands executing on the device. After modifying the value of WP_n, the host shall not issue a new command to the device for at least tWW delay time.

The figure below describes the tWW timing requirement, shown with the start of a Program command. The bus shall be idle for tWW time after WP_n transitions from zero to one before a

new command is issued by the host, including Program. The bus shall be idle for tWW time after WP_n transitions from one to zero before a new command is issued by the host.

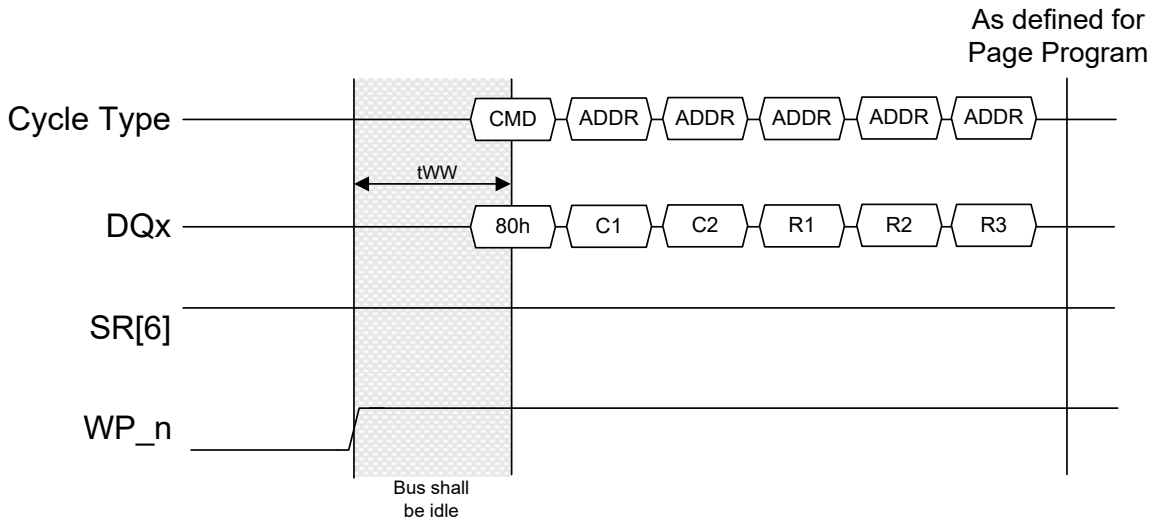


Figure 2-21 Write Protect timing requirements example

2.15. Volume Appointment

Volume Addressing and Volume Appointment for Matrix ODT operation are only used in the Conv. Protocol. This section is not applicable for the SCA Protocol.

Figure 2-22 shows an example of a multi-package channel topology where the use of Non-Target ODT may be useful. If the host wants to have the terminator on a package that does not share a CE_n with the selected NAND Target, then each NAND Target that may act as a terminator shall have a Volume appointed at initialization using the Set Features command to the Volume Configuration feature.

Each CE_n shall be individually pulled low and have a unique Volume Address appointed. Once all NAND Targets have Volume Addresses appointed, the appointed Volume Addresses may be used for termination selection.

During operation, the CE_n signal for the selected Volume and for any NAND Targets assigned as a terminator for the selected Volume need to be brought low. When CE_n is brought low for an unselected Volume, all LUNs that are not assigned as terminators for the selected Volume are deselected.

After Volume Addresses have been appointed to LUNs on a CE_n, the Volume Select command need to be used to select and deselect the Volumes on the channel. For more efficient issuance of Volume Select commands, multiple CE_n may be asserted on the channel during Volume Select sequence issuance to simultaneously select and deselect Volumes.

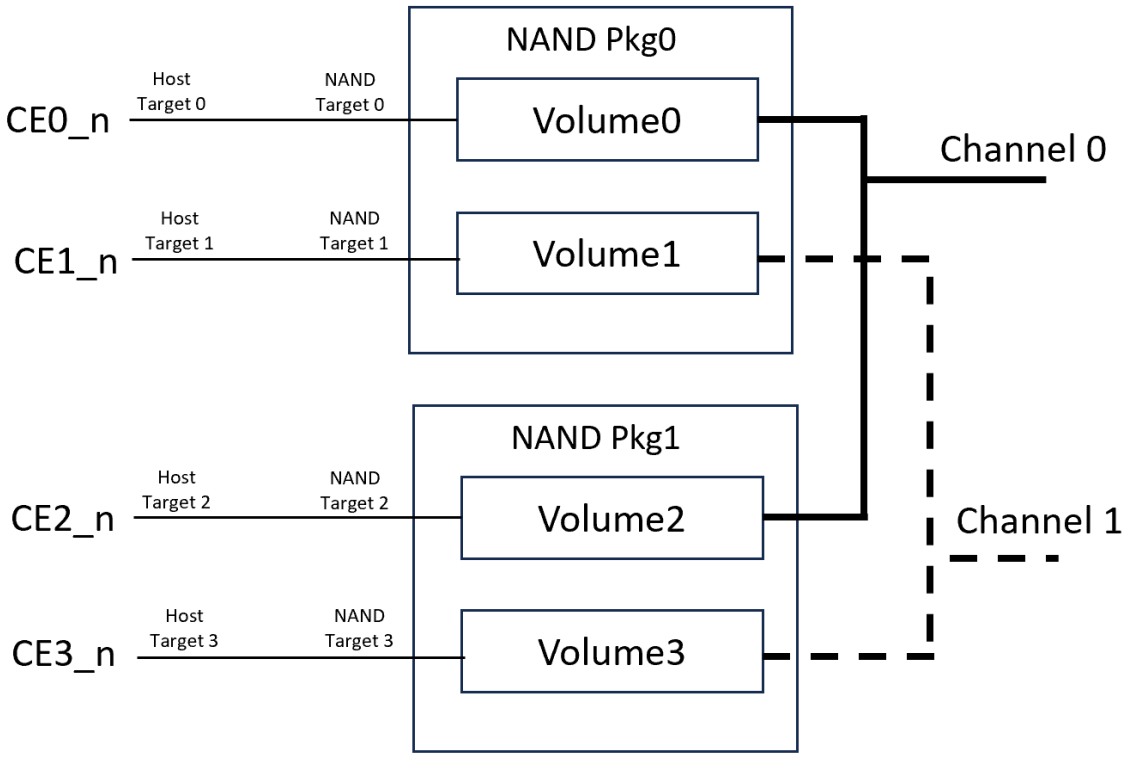


Figure 2-22 Example Multi-Package Channel Topology

3. Memory Organization

Figure 3-1 shows an example of a Target memory organization. In this case, there are two logical units where each logical unit has two planes.

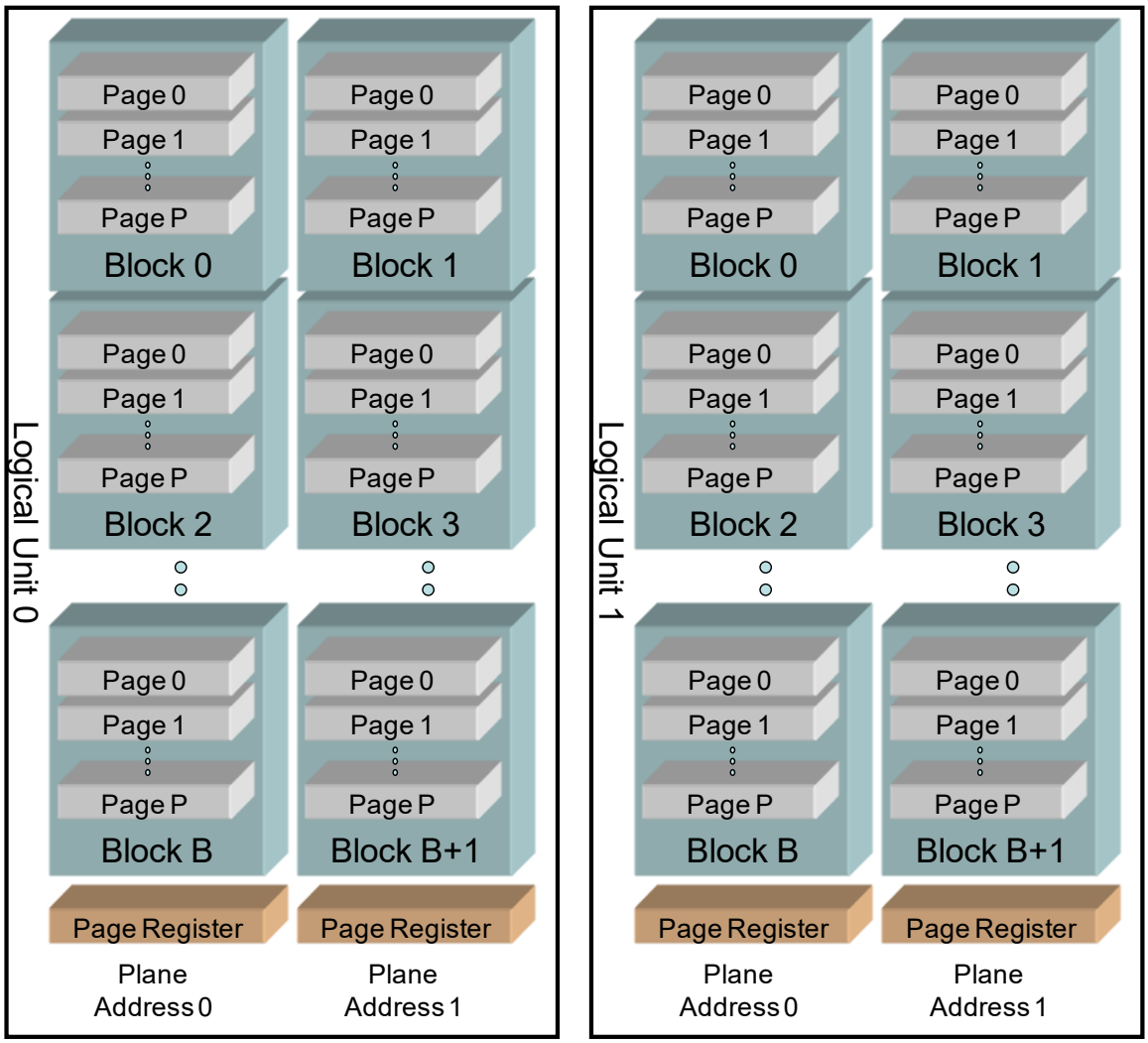


Figure 3-1 Target Memory Organization

A device contains one or more targets. A target is controlled by one CE_n signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. See multiple LUN operation restrictions in section 3.1.3.

A LUN shall contain at least one page register. The number of page registers is dependent on the number of multi-plane operations supported for that LUN. A page register is used for the

temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The Flash array on a LUN contains a number of blocks.A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN.

A block contains a number of pages. A page is the smallest addressable unit for read and program operations. A page consists of a number of bytes or words. The number of user data bytes per page, not including the spare data area, shall be a power of two. The number of pages per block shall be a multiple of 32.

The byte or word location within the page register is referred to as the column.

There are two mechanisms to achieve parallelism within this architecture. There may be multiple commands outstanding to different LUNs at the same time. To get further parallelism within a LUN, multi-plane operations may be used to execute additional dependent operations in parallel.

3.1. Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes or words within a page, i.e. the column address is the byte/word offset into the page. The least significant bit of the column address shall always be zero (i.e., an even number of bytes is always transferred). The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, like Block Erase. In this case the column addresses are not issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in the figure below with the least significant row address bit to the right and the most significant row address bit to the left.

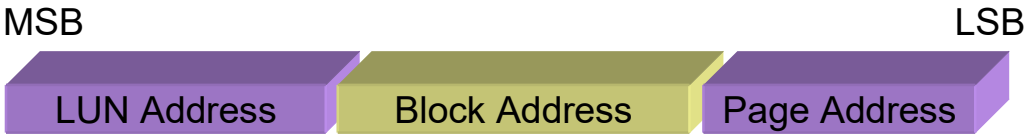


Figure 3-2 Row Address Layout

The number of blocks and number of pages per block is not required to be a power of two. In the case where one of these values is not a power of two, the corresponding address shall be rounded to an integral number of bits such that it addresses a range up to the subsequent power of two value. The host shall not access upper addresses in a range that is shown as not supported. For example, if the number of pages per block is 96, then the page address shall be rounded to 7 bits such that it can address pages in the range of 0 to 127. In this case, the host shall not access pages in the range from 96 to 127 as these pages are not supported.

The page address always uses the least significant row address bits. The block address uses the middle row address bits and the LUN address uses the most significant row address bit(s).

3.1.1. Multi-Plane Addressing

The multi-plane address comprises the lowest order bits of the block address as shown in Figure 3-3. The following restrictions apply to the multi-plane address when executing a multi-plane command sequence on a particular LUN:

- The plane address bit(s) shall be distinct from any other multi-plane operation in the multi-plane command sequence.
- Some devices or multi-plane operations may require page addresses to be the same as other multi-plane operations in the multi-plane command sequence. Refer to the vendor datasheet for the multi-plane operation restrictions applicable to the device.

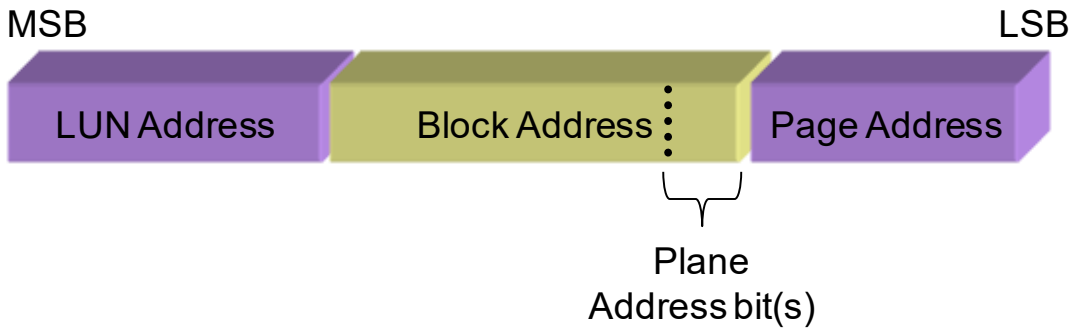


Figure 3-3 Plane Address Location

3.1.1.1. Multi-Plane Block Address Restrictions

The device may indicate multi-plane block address restrictions. The specific cases are:

- No restriction: All block address bits may be different between two plane addresses.
- Full restriction: All block address bits (other than the plane address bits) shall be the same between two plane addresses.
- Lower bit XNOR restriction: If the XNOR of the lowest plane address bits (bit 0) is one between two plane addresses, then there is a full restriction between these two plane addresses. If the XNOR of the lower plane address bits is zero between two plane addresses, then there is no restriction between these two plane addresses.

The table below illustrates the three types of restrictions for a four-plane operation:

Restriction Type	Plane Address 0	Plane Address 1	Plane Address 2	Plane Address 3
No restriction	Block A	Block B	Block C	Block D
XNOR restriction	Block A	Block B	Block A+2	Block B+2
Full restriction	Block A	Block A+1	Block A+2	Block A+3

Table 3-1 Four-plane address restriction

The table below describes whether there is a lower bit XNOR restriction between two plane addresses A and B, based on their plane address bits for a 4-plane implementation. If there is a

lower bit XNOR restriction, then the block addresses (other than the plane address bits) shall be the same between multi-plane addresses A and B.

Multi-plane Address bits A	Multi-plane Address bits B	Lower Bit XNOR	XNOR Restriction Between A and B
00b	01b	0 XNOR 1 = 0	No
00b	10b	0 XNOR 0 = 1	Yes
00b	11b	0 XNOR 1 = 0	No
01b	10b	1 XNOR 0 = 0	No
01b	11b	1 XNOR 1 = 1	Yes
10b	11b	0 XNOR 1 = 0	No

Table 3-2 4-way lower bit XNOR restriction

3.1.2. Logical Unit Selection for Data Output

Logical units that are part of a NAND Target share a single data bus with the host. The host shall ensure that only one LUN is selected for data output to the host at any particular point in time to avoid bus contention.

The host selects a LUN for future data output by issuing a Read Status Enhanced command to that LUN. The Read Status Enhanced command shall deselect the output path for all LUNs that are not addressed by the command. The page register selected for output within the LUN is determined by the previous Read (Cache) commands issued and is not impacted by Read Status Enhanced.

3.1.3. Multi-LUN Operation Restrictions

The Multi-LUN operation restrictions described in this section only apply to the Conv. Protocol. See the SCA Protocol section for Multi-LUN operation restrictions for the SCA Protocol.

LUNs are independent entities. A multiple LUN operation is one in which two or more LUNs are simultaneously processing commands. During multiple LUN operations the individual LUNs involved may be in any combination of busy or ready status

When a Page Program command (80h) is issued on any LUN that is not preceded by an 11h command, all idle LUNs may clear their page registers if the program page register clear enhancement is not supported or enabled. Thus, the host should not begin a Page Program command on a LUN while a Read Page operation is either ongoing or has completed but the data has not been read from another LUN, as the contents of the page register for the Read operation are lost. If the program page register clear enhancement is enabled, this restriction does not apply. A Read Page can be issued to one LUN while a Page Program is ongoing within a second LUN without any restriction.

When issuing a Page Program command (80h), the host should not select another LUN within the same Volume until after all data has been input and a 10h or 15h command has been issued. In the case of multi-plane operations, all data input for all multi-plane addresses should be completed prior to selecting another LUN.

When issuing Reads to multiple LUNs, the host shall take steps to avoid issues due to column address corruption. The host shall issue a Change Read Column or Change Read Column Enhanced before starting to read out data from a newly selected LUN.

If a multi-LUN operation has been issued, then the next status command issued shall be Read Status Enhanced. Read Status Enhanced causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Read Status Enhanced command responds to a subsequent data output cycle. After a Read Status Enhanced command has been completed, the Read Status command may be used until the next multiple LUN operation is issued.

When the host has issued Read Page commands to multiple LUNs at the same time, the host shall issue Read Status Enhanced before reading data from either LUN. This ensures that only the LUN selected by the Read Status Enhanced command responds to a data output cycle after being put in data output mode with a 00h command, and thus avoiding bus contention (NOTE: Some NAND vendors may require the use of Change Read Column Enhanced sequence instead of 00h command to output data from the NAND, see vendor datasheet). A Change Read Column Enhanced command is required for any LUN that Read Page commands are outstanding for prior to transferring data from that LUN that is part of the multiple LUN read sequence. An example sequence is shown below:

1) Read Page command issued to LUN 0
2) Read Page command issued to LUN 1
3) Read Status Enhanced selects LUN 0
4) Change Read Column Enhanced issued to LUN 0
5) Data transferred from LUN 0
6) Read Status Enhanced selects LUN 1
7) Change Read Column Enhanced issued to LUN 1
8) Data transferred from LUN 1

When issuing mixed combinations of commands to multiple LUNs (e.g. Reads to one LUN and Programs to another LUN), after the Read Status Enhanced command is issued to the selected LUN a Change Read Column or Change Read Column Enhanced command shall be issued prior to any data output from the selected LUN.

Support for Read Status Enhanced followed by Change Read Column is optional and a NAND vendor may require the use of either Change Read Column Enhanced command or a Read Status Enhanced command followed by a Change Read Column Enhanced sequence, instead. Refer to the vendor datasheet.

3.2. Volume Addressing (Conv. Protocol Only)

Volume Addressing and Volume Appointment for Matrix ODT operation are only used in the Conv. Protocol. This section is not applicable for the SCA Protocol.

3.2.1. Appointing Volume Address

To appoint a Volume Address, the Set Feature command is issued with a Feature Address for Volume Configuration. The Volume address is not retained across power cycles, and thus if Volume Addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s).

3.2.2. Selecting a Volume

After Volume Addresses have been appointed, to select a NAND Target, the associated CE_n for that NAND Target must first be de-asserted HIGH for a minimum time of tCEH, after which the

CE_n may then be pulled low, then the host issue a Volume Select command with the address of the Volume that shall execute the next command issued.

3.2.3. Multiple Volume Operations Restrictions

Volumes are independent entities. A multiple Volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected Volume, CE_n shall be pulled high for a minimum of tCEH and the Volume Select command shall then be issued to select the Volume to issue a command to next. While commands (including multi-LUN operations) are being performed on the selected Volume, a Volume Select command is not required.

Issuing the same command to multiple Volumes at the same time is not supported.

For a LUN-level command (e.g. Read, Program), the host may select a different Volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN-level command, however for devices that support >800 MT/s, when interrupting data input operations with a Volume Select command, the host may be required to issue an 11h command prior to the Volume Select command (see vendor datasheet). When re-selecting a Volume and the associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall wait tCCS and then issue a Change Row Address command prior to resuming data input. If Change Row Address is not supported, then all data shall be transferred before selecting a new Volume.
- Data output: The host shall issue a Change Read Column Enhanced or Random Data Out command prior to resuming data output. If neither of these commands are supported, then all data shall be transferred before selecting a new Volume.

For a Target-level command (e.g. Get Features, Set Features), the host shall complete all data input or data output operations associated with that command prior to selecting a new Volume.

A Volume Select command shall not be issued during the following atomic portions of the Read, Program, Erase, and Copyback operations:

- Read (including Copyback Read)
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 30h>
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 31h>
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 32h>
  - <CMD: 00h> <ADDR: Column & Row> <CMD: 35h>

- Program (including Copyback Program) **NOTE:** The Volume Select command may be issued prior to the 10h, 11h, or 15h command if the next command to this Volume is Change Row Address, however for devices supporting >800 MT/s, an 11h command may be required prior to the Volume Select command (see vendor datasheet). After Volume Select command is issued to resume data input, the host shall wait tCCS before issuing Change Row Address command.
  - <CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
  - <CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
  - <CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>
  - <CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
  - <CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
  - <CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>
  - <CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
  - <CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
  - <CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>

- Erase
  - <CMD: 60h> <ADDR: Row> <CMD: D0h>
  - <CMD: 60h> <ADDR: Row> <CMD: D1h>
  - <CMD: 60h> <ADDR: Row> <CMD: 60h> <ADDR: Row> <CMD: D1h>

3.2.4. Volume Reversion

When using Volume Addressing, the LUNs shall support Volume reversion. Specifically, if CE_n is transitioned from high to low and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states (defined in Table 4-24) based on the last specified Volume address.

The figure below defines the Volume reversion requirements when CE_n transitions from high to low.

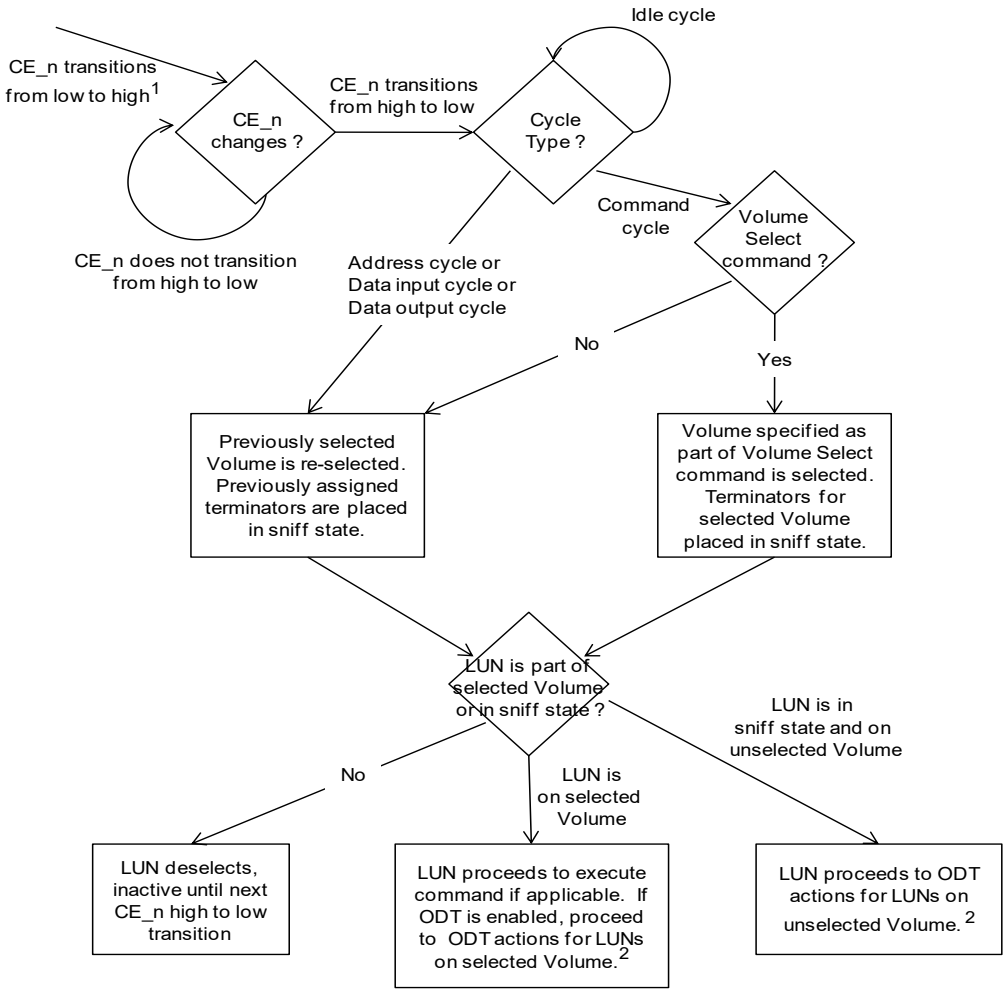


Figure 3-4 Volume Reversion Behavioral Flow

NOTE:
1. This state is entered asynchronously when CE_n transitions from low to high.
2. ODT actions for LUNs on a selected Volume are specified in Figure 4-15

3. ODT actions for LUNs on an unselected Volume are specified in Figure 4-16

3.3. Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects may be present that renders some blocks unusable. Block granularity is used for mapping factory defects since those defects may compromise the block erase capability.

Two methods for identifying Factory Bad Blocks (FBBs) are described in this document:
a) FBB Scan via Bad Block Mark (legacy method for identifying FBBs)
b) FBB Scan via Read Status (new method for identifying FBBs)

It is NAND vendor specific which method among the above-mentioned methods for FBB identification is supported by a NAND device.

3.3.1. FBB Scan via Bad Block Mark (Optional)

This is the legacy method for identifying FBBs on a NAND device. The requirements for this method are described in the following subsections:

3.3.1.1. FBB Scan via Bad Block Mark Device Requirements

If a block is defective and 8-bit data access is used, the manufacturer shall mark the block as defective by setting the first byte in the defect area, as shown in the figure below, of the first or last page of the defective block to a value of 00h. If a block is defective and 16-bit data access is used, the manufacturer shall mark the block as defective by setting the first word in the defect area of the first or last page of the defective block to a value of 0000h.

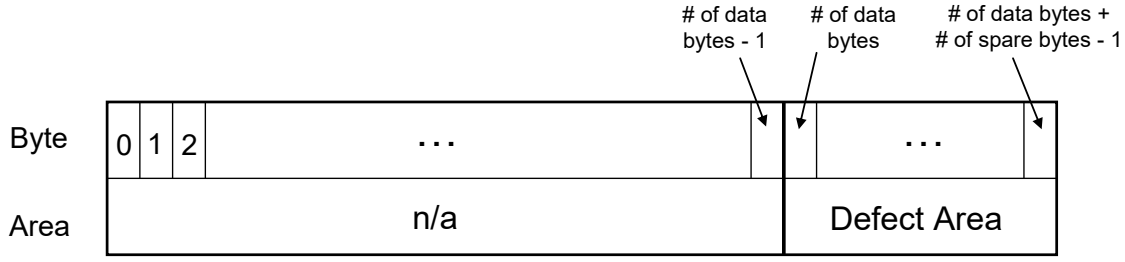


Figure 3-5 Area marked in factory defect mapping

3.3.1.2. FBB Scan via Bad Block Mark Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure 3-6 outlines the algorithm to scan for factory mapped defects. This algorithm should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The initial state of pages in non-defective blocks is vendor specific although the data at the locations of the bad block mark for non-defective blocks shall not be 00h. A defective block is indicated by a byte value equal to 00h for 8-bit access or a word value equal to 0000h for 16-bit access being present at the first byte/word location in the defect area of either the first page or last page of the block. The host shall check the first byte/word of

the defect area of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE: Over the lifetime use of a NAND device, the defect area of defective blocks may encounter read disturbs that cause values to change. The manufacturer defect markings may change value over the lifetime of the device and are expected to be read by the host and used to create a bad block table during initial use of the part.

```
for (i=0; i<NumLUNs; i++)
{
      for (j=0; j<BlocksPerLUN; j++)
      {
            Defective=FALSE;

            ReadPage(lun=i; block=j; page=0; DestBuff=Buff);
            if (Buff[PageSize] == 00h)  // Value checked for is 0000h for 16-bit access
                  Defective=TRUE;

            ReadPage(lun=i; block=j; page=PagesPerBlock-1; DestBuff=Buff);
            if (Buff[PageSize] == 00h)  // Value checked for is 0000h for 16-bit access
                  Defective=TRUE;

            if (Defective)
                  MarkBlockDefective(lun=i; block=j);
      }
}
```

Figure 3-6 Factory defect bad block mark scanning algorithm

3.3.2. FBB Scan via Read Status (Optional)

The host may check for factory bad blocks (FBB) by performing a read status check after a valid FBB algo operation to a block. If the FAIL status bit is set (e.g., SR[0]=1), the block is a bad block.

For this method, the valid FBB algo operations are:

a) A single-plane page read to the 1st page of the block, or
b) A single-plane block erase to the block

It is NAND vendor specific whether a device supports one or both of the above valid FBB algo operations for checking for FBBs.

After a valid FBB algo operation, a Read Status or Read Status Enhanced sequence may be used to check the FAIL status bit value (see NAND vendor datasheet if only one or both Read Status and Read Status Enhanced are supported for checking FAIL status bit value after the valid FBB algo operation).

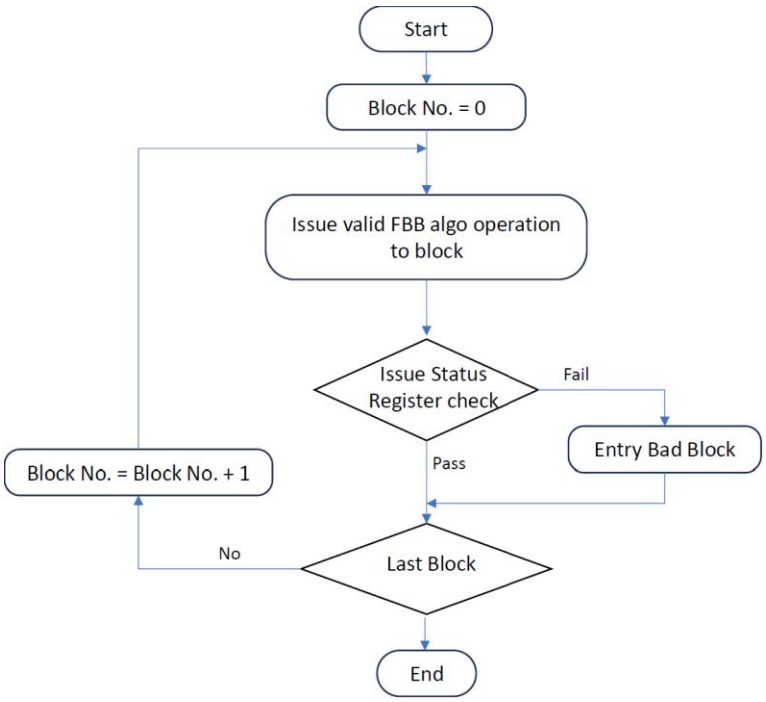


Figure 3-7 FBB Scan via Read Status Check Example

3.4. Discovery and Initialization

3.4.1. Multiple CE_n

There may be multiple chip enable (CE_n) signals on the controller channel, one for each separately addressable target. To determine the targets that are connected, the procedure outlined in this section shall be followed for each distinct CE_n signal.

CE_n signals shall be used sequentially on the device; CE0_n is always connected and CE_n signals shall be connected in a numerically increasing order. The host shall attempt to enumerate targets connected to all host CE_n signals.

3.4.1.1. Single Data Bus Discovery

The CE_n to test is first pulled low by the host to enable the target if connected, while all other CE_n signals are pulled high. The host shall then issue the Reset (FFh) command to the target. Following the reset, the host should then issue a Read ID command to the target. If the ONFI signature is returned by the Read ID command with address 20h, then the corresponding target is connected. If the ONFI signature is not returned or any step in the process encountered an error/timeout, then the CE_n is not connected and no further use of that CE_n signal shall be done.

3.4.1.2. Dual/Quad Data Bus Discovery

The CE_n to test is first pulled low by the host to enable the target if connected, while all other CE_n signals are pulled high. The host shall then issue the Reset (FFh) command to the target.

Following the reset, the host should then issue a Read ID command with address 20h to the target. If the ONFI signature is returned by the Read ID command, then the corresponding target is connected.

If the ONFI signature is not returned (or any step in the process encountered an error/timeout), then the second 8-bit data bus should be probed. The host shall issue the Reset (FFh) command to the target using the second 8-bit data bus. Following the reset, the host should then issue a Read ID command with address 20h to the target on the second 8-bit data bus. If the ONFI signature is returned by the Read ID command, then the corresponding target is connected and is using the second 8-bit data bus. After discovering that the target is using the second 8-bit data bus, all subsequent commands to that target shall use the second 8-bit data bus including Read Parameter Page. If the ONFI signature is not returned for the second 8-bit data bus, the discovery process described for the second 8-bit data bus should be repeated for the third and fourth 8-bit data busses.

If after this point a valid ONFI signature is not discovered or further errors were encountered, then the CE_n is not connected and no further use of that CE_n signal shall be done.

3.4.2. Target Initialization

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE_n signal, including performing the Read Parameter Page (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the Read Parameter Page (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid (refer to section 6.7.1.42), the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. All parameter pages returned by the Target may have invalid CRC values; however, bit-wise majority or other ECC techniques may be used to recover the contents of the parameter page. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present (refer to section 6.7.1.1), then all parameter pages have been read.

The Read ID and Read Parameter Page commands only use the lower 8-bits of the data bus. The host shall not issue commands that use a word data width on x16 devices until the host determines the device supports a 16-bit data bus width in the parameter page.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

4. Data Interface and Timing

4.1. Data Interface Overview

A summary of the interface characteristics for ONFI 6.0 NAND devices is shown below:

Feature	NV-LPDDR4 (LTT) (Required)	NV-LPDDR4 with VccQL (PI-LTT) (Optional)
Data clocking	Double data rate (DDR)	Double data rate (DDR)
Maximum Speed	4800[1] MT/s	4800[1] MT/s
Volume Addressing support	Yes on Conv. Protocol, No on SCA Protocol	Yes on Conv. Protocol, No on SCA Protocol
On-die termination support	Yes	Yes
Differential signaling	Yes, required for DQS and RE_n	Yes, required for DQS and RE_n
Vcc	2.5V	2.5V
VccQ	1.2V	1.2V
VccQL	1.2V required on ”VccQ or VccQL” balls/pads	0.6V required on “VccQ or VccQL” balls/pads
External Vpp support	Yes	Yes
External VREFQ support	No	No
ZQ Calibration	Yes, required	Yes, required
Input Path Topology	Unmatched DQS	Unmatched DQS
Differential Signaling enabled on Power-up	Yes	Yes
Equalization (DFE)	DFE 1-tap (required) DFE 4-tap (optional)	DFE 1-tap (required) DFE 4-tap (optional)
Training Features	Write/Read DQ Training, DCC, Internal VrefQ,WDCA, RDCA, Write Training Monitor, Per-pin VrefQ Adjustment, DQS Oscillator	Write/Read DQ Training, DCC, Internal VrefQ,WDCA, RDCA, Write Training Monitor, Per-pin VrefQ Adjustment, DQS Oscillator

Notes:
1. The maximum timing mode a NAND device supports is vendor specific (See vendor datasheet)

Table 4-1 Data Interface Comparison

Feature		Data Rate (MT/s)					
		~200	~400	~800	~1200, ~1600, ~1800, ~2000, ~2200, ~2400	~2800, ~3200	~3600, ~4000, ~4400, ~4800
VccQ		1.2V					
VccQL (PI-LTT)	NAND	0.6V (Optional)					
	Host	0.6V (Optional)					

I/O Type	Single-ended Signaling for DQS and RE [1]	NAND	Not supported	Not supported
		Host	Not supported [7]	
	Differential Signaling for DQS and RE	NAND	Supported	
		Host	Required	
ZQ Calibration		NAND	Supported	
		Host	Required [2]	Required
Training (DCC)		NAND	Not supported	Required
		Host		
Training (Read)		NAND	Supported	
		Host	Optional	Required
Training (Write)		NAND	Supported	
		Host	Required	
Training (WDCA)		NAND	Optional	Supported
		Host	Optional	Required
Training (RDCA)		NAND	Optional	Optional
		Host	Optional	Supported
Training (Per-Pin VrefQ via FA 40h/41h)		NAND	Optional	Supported
		Host	Optional	Required
Training (Internal VrefQ via FA 23h)		NAND	Supported	
		Host	Required	
On-Die Termination	NV-DDR3 (CTT)	NAND	Not Supported [3]	
		Host	Not Supported [2]	
	NV-LPDDR4 (LTT)	NAND	Supported	
		Host	Optional [4]	
	NV-LPDDR4 with VccQL (PI-LTT) (Optional)	NAND	Optional	
		Host	Optional [4]	
Internal VrefQ	NV-LPDDR4 (LTT)	NAND	Supported [5]	
		Host	Supported [5]	
	NV-LPDDR4 with VccQL (PI-LTT) (Optional)	NAND	Supported [5]	
		Host	Supported [5]	

Equalization (DFE)	NAND	Optional and Vendor Specific		Supported
	Host			Required
DQS Oscillator	NAND	Optional and Vendor Specific		Supported
	Host			Supported
Pausing Data Input/Output	NAND	Optional	Not supported	
	Host	Optional	Not supported	
Warm-up Cycles	NAND	Optional	Supported	
	Host	Optional	Supported	Required
Conv. Protocol (command/address)	NAND	Optional [6]		
	Host	Optional		
SCA Protocol (command/address)	NAND	Required		
	Host	Supported		

NOTES:

- Optional = Host or NAND can Support or Not Support
- Supported = Host or NAND supports feature but may not be required to use (dependency on application)
- Required = Host or NAND is required to support feature and required to use the feature

1) For NV-LPDDR4 mode, Differential Signaling is always required, even below 200Mbps.
2) Optional for controllers that also support NV-DDR3 (CTT) capable NAND devices.
3) Supported on ONFI 5.2 and earlier NAND devices, not supported on ONFI 6.0 NAND devices.
4) Host can enable/disable On Die (NAND) Termination.
5) The NAND shall power-up with the NV-LPDDR4 (LTT) interface enabled and with internal VrefQ. The host shall ensure that the NAND internal VrefQ is within the NAND minimum internal VrefQ allowable range allowed for the NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT) interface prior to enabling the NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT) interface, and at any time while the NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT) interface is active. External VrefQ shall always be disabled when the device runs in NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT) modes.
6) Conventional protocol might not be supported on later NAND devices.
7) ONFI 6.0 compliant NAND controllers are required to power-up with differential DQS/RE for data input enabled (i.e., controller driving DQS_t, DQS_c, RE_t and RE_c signals to their default states). However, to enable backward compatibility with ONFI 5.2 and earlier NAND devices (which can power-up with single-ended DQS/RE), it is recommended that ONFI 6.0 controllers, use single-ended DQS when read data from the NAND as power-up default (i.e., use DQS_t and ignore DQS_c) and provide a controller setting to enable using DQS_c for NAND reads at a later time.

Table 4-2 Supported Features and Operating Conditions Versus Data Rate

On power up, the device shall operate in timing mode 0. After the host determines the timing modes supported in the parameter page, the host may enable the supported timing mode by transitioning CE_n high and changing the interface speed to the desired timing mode. The new timing mode is active when the host pulls CE_n low.

The NV-LPDDR4 data interface (with and without VccQL) uses a DDR protocol. Thus, an even number of bytes is always transferred. The least significant bit of the column address shall always

be zero when using the DDR protocol. If the least significant bit of the column address is set to one when using the DDR protocol, then the results are indeterminate.

4.2. Conv. Protocol Bus States

4.2.1. Conv. Protocol Bus State Table

CE_n	ALE	CLE	RE_n5 (RE_t)	DQS (DQS_t)	WE_n	Data Input or Output[1]	Measurement Point	Bus State
1	X	X	X	X	X	X	X	Standby
0	0	0	1	1	1	None	X	Idle
0	0	1	1	1[6]		None	WE_n rising edge to rising edge	Command cycle
0	1	0	1	1[6]		None	WE_n rising edge to rising edge	Address cycle
0	0	0	1		1	Input	DQS rising edge to rising edge	Data input cycle[2,3]
0	0	0			1	Output	RE_n rising edge to rising edge	Data output cycle[2,3,4]

NOTE:
1. The current state of the device is data input, data output, or neither based on the commands issued.
2. There are two data input/output cycles from the rising edge of DQS/RE_n to the next rising edge of DQS/RE_n.
3. ODT may be enabled as part of the data input and data output cycles.
4. At the beginning of a data output burst, DQS shall be held high for tDQSRH after RE_n transitions low to begin data output.
5. RE and DQS complementary signals are mandatory for NV-LPDDR4 (with or without VccQL)
6. DQS is recommended to be 1 during command cycles, except in the case where a data input burst is terminated with a CLE=1 and a confirm command is issued, where DQS must be held LOW to meet tWPSTH and tCDQSH requirements. DQS is also recommended to be 1 during address cycles.

Table 4-3 Bus State Table

4.2.2. Conv. Protocol Pausing Data Input/Output and Restarting an Exited Data Input/Output Sequence

The host may pause data input or data output by entering the Idle state when using any data interface.

Pausing of data output may be done in the middle of a data output burst by pausing RE_n (RE_t/RE_c) and holding the signal(s) static high or low until the data burst is resumed. The pausing of data input may also be done in the middle of a data input burst by pausing DQS (DQS_t/DQS_c) and holding the signal(s) static high or low until the data burst is resumed. The data burst can be considered paused if DQS (DQS_t/DQS_c) or RE_n (RE_t/RE_c) is paused such that the current I/O frequency is not maintained for the data burst. WE_n shall be held high during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause.

Pausing in the middle of a data input or data output burst however, is only allowed up to the 800MT/s data rate. Above 800MT/s, for signal integrity reasons, pausing in the middle of a data input or data output burst is not allowed, and if the data burst is interrupted, the host is required to exit first the data burst prior to resuming it.

A data burst is exited when either ALE or CLE or CE_n is toggled to a 1. After a data burst has been exited, if warmup cycles are enabled, then warmup cycles are required when re-starting the data burst. After a data burst has been exited, ODT also may be disabled, however if needed to meet the signal integrity needs of the system, ODT must be re-enabled prior to re-starting the data burst. If the host desires to end the data burst, after exiting the data burst, a new command is issued.

The figure below is an example of exiting a data input burst with a CLE=1 and resuming the data input burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data input burst is resumed.

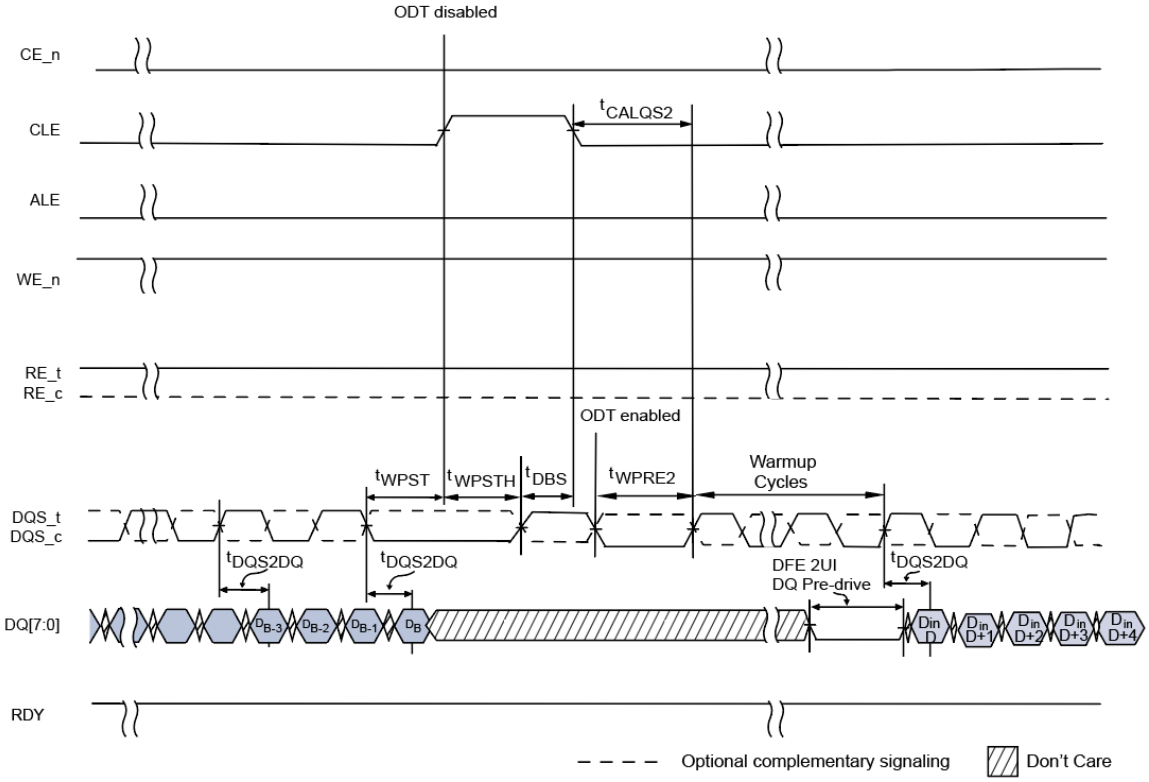


Figure 4-1 Example of Data Input Burst Exit with CLE=1 and Resume with CLE=0

The figure below is an example of exiting a data output burst with a CLE=1 and resuming the data output burst with a CLE=0. Warmup cycles if enabled are required to be issued when the data output burst is resumed.

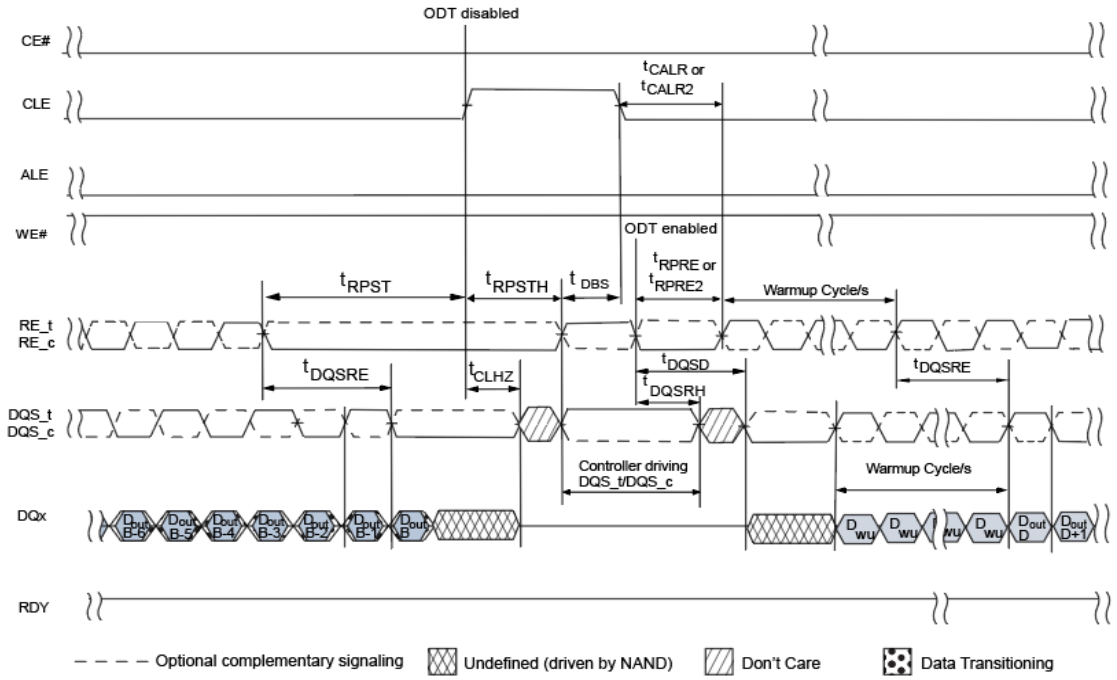


Figure 4-2 Example of Data Output Burst Exit with CLE=1 and Resume with CLE=0

As shown in Figure 4-3, for devices that support >800 MT/s, if the data input burst is exited (with a CLE or ALE or CE_n high) and CE_n is held high for >1us, in order to be able to resume the data input burst at a later time, the host may be required to issue a vendor specific command (e.g. 11h) prior to exiting the data input burst (see vendor datasheet). To restart an exited data input burst where the CE_n has been held high for >1us, a Change Write Column or Change Row Address command shall be issued (see vendor datasheet if both commands or only one of those commands are supported in resuming the data input burst).

As shown in Figure 4-4, for devices that support >800 MT/s, if the data output burst is exited (with a CLE or ALE or CE_n high) and CE_n is held high for >1uS, in order to restart an exited data output burst, the host may be required to issue a Change Read Column or Change Read Column Enhanced command (see vendor datasheet).

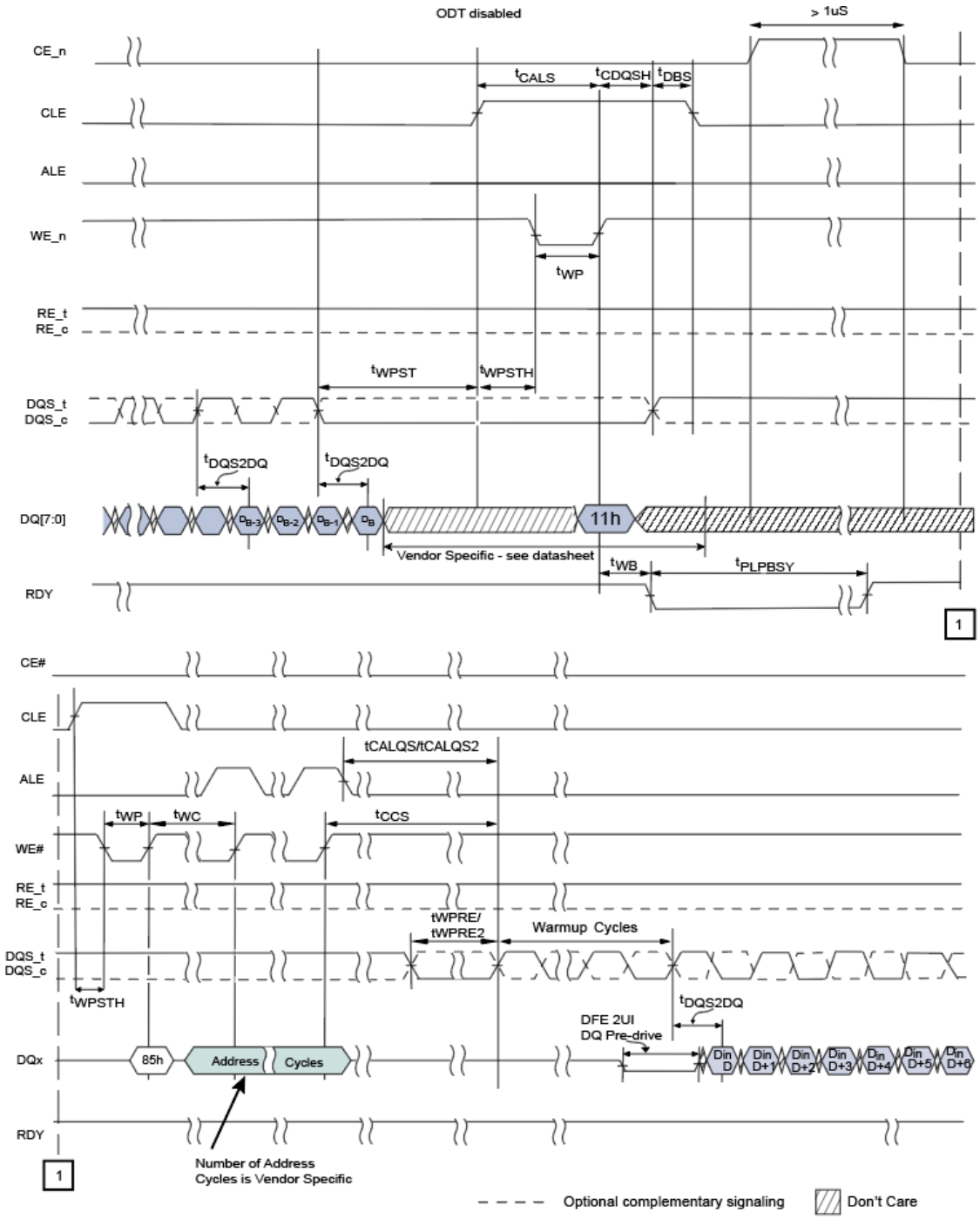


Figure 4-3 Example of Data Input Burst Exit with CE_n High > 1uS and Resume Sequence for Devices that support greater than 800 MT/s

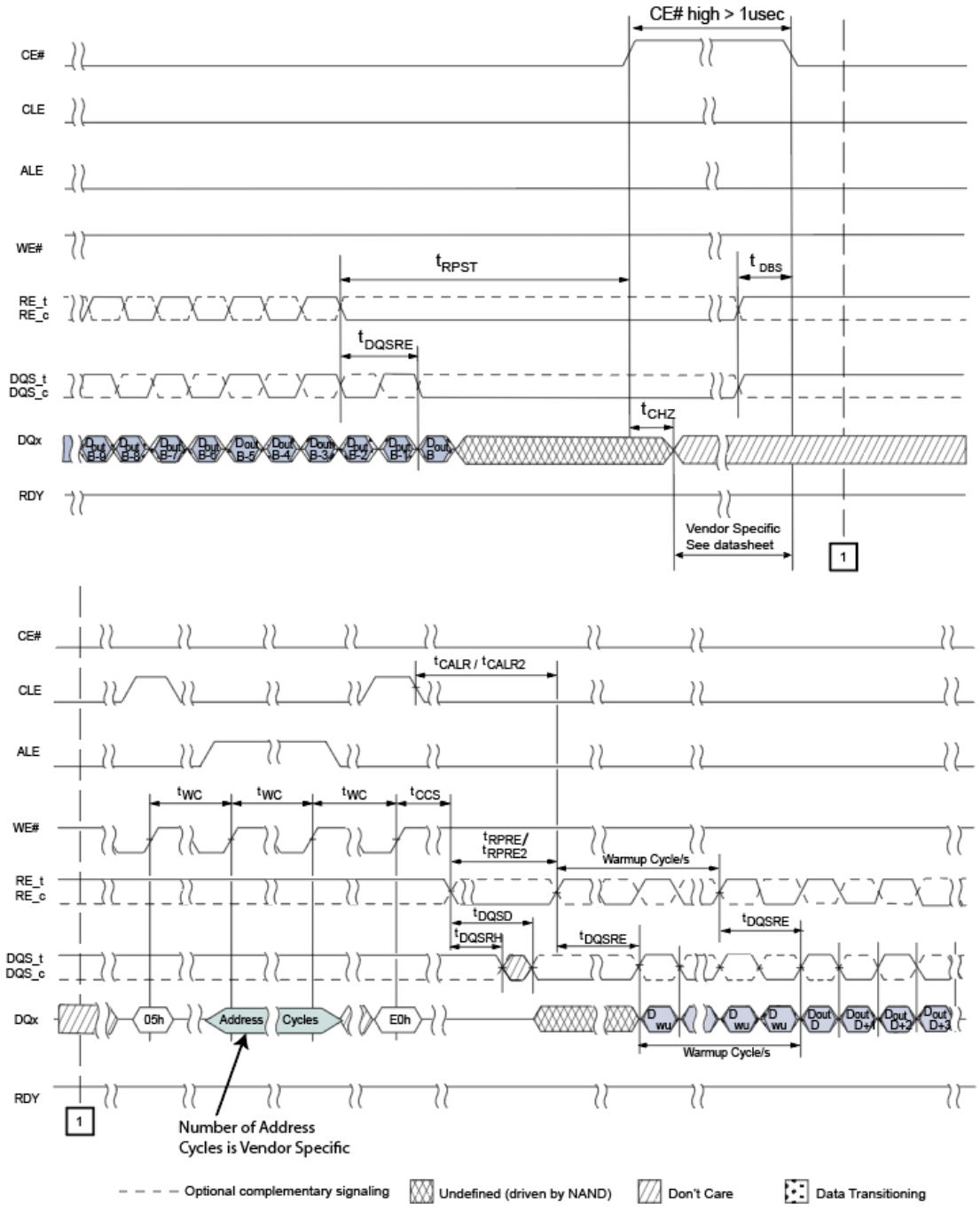


Figure 4-4 Example of Data Output Burst Exit with CE_n High > 1uS and Resume Sequence for Devices that Support greater than 800 MT/s

4.3. Conv. Protocol Repeat Bytes

The NV-LPDDR4 data interface (with and without VccQL) uses the DDR data transfer technique to achieve a high data transfer rate. However, certain configuration and settings commands are

not often used and do not require a high data transfer rate. Additionally, these commands typically are not serviced by the pipeline used for data transfers.

To avoid adding unnecessary complexity and requirements to implementations for these commands, the data is transferred using single data rate. Specifically, the same data byte is repeated twice and shall conform to the timings required for the NV-LPDDR4 data interface. The data pattern in these cases is D_0 D_0 D_1 D_1 D_2 D_2 etc. The receiver (host or device) shall only latch one copy of each data byte. Data input or data output, respectively, shall not be paused during these commands. The receiver is not required to wait for the repeated data byte before beginning internal actions.

The commands that repeat each data byte twice in the NV-LPDDR4 data interface are: Set Features, Read ID, Get Features, Read Status, Read Status Enhanced, and ODT Configure. SDR commands may use the highest data transfer rate supported by the device. If an ODT Configure command is not issued using SDR timing mode 0 then host shall wait 40ns prior to issuing the next command cycle.

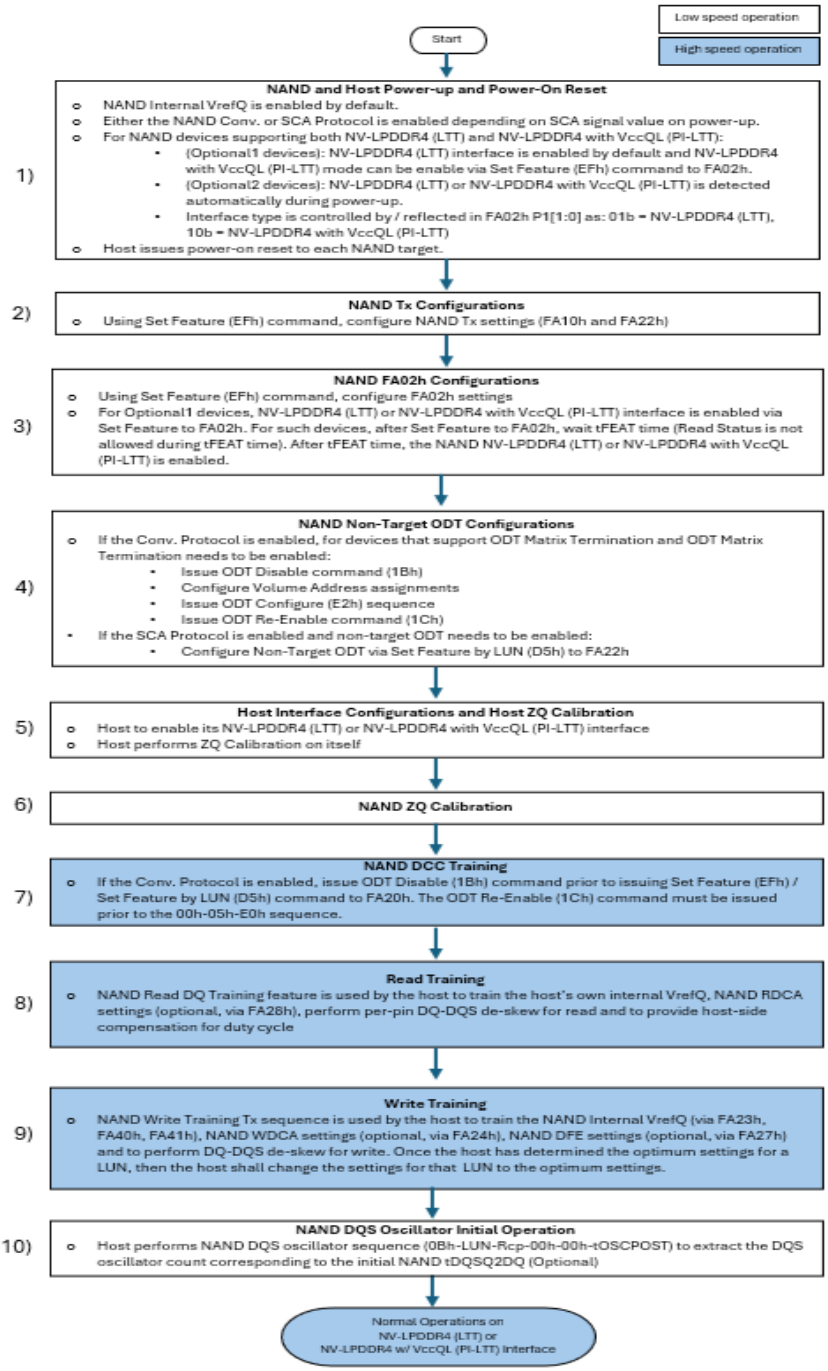
4.4. Timing Mode Transitions

When the Conv. Protocol is enabled, to change the timing mode, the host should transition CE_n high and change the interface speed to the desired timing mode. The new timing mode is active when the host pulls CE_n low. Prior to issuing any new commands to the device, the host shall transition CE_n high.

When the SCA Protocol is enabled, to change the timing mode for the DQ bus, the host shall first terminate any active data burst (data burst that has been started with an SCE packet and not yet terminated by an SCT packet) on the old timing mode with an SCT packet. Succeeding data bursts on the DQ bus may then be done with the new timing mode.

4.5. Interface Initialization

The host shall follow the initialization flow shown in the following figure:



Notes:

1) ODT Disable (1Bh) and ODT Re-Enable (1Ch) commands shall be used for Set Feature (EFh) / Set Feature by LUN (D5h) commands between steps 3) and 9). Issue ODT Disable (1Bh) command prior to issuing Set Feature (EFh) / Set Feature by LUN (D5h) command and issue ODT Re-Enable (1Ch) after the Set Feature (EFh) / Set Feature by LUN (D5h).

Figure 4-5 NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT) Initialization Flow

4.6. Data Bus Inversion

4.6.1. DBI Purpose and Function

Data Bus Inversion (DBI) is an optional function for NAND device to reduce power consumption and power/bus noise during data input/output. A device supporting DBI shall have DBI pin to designate if the DQ signals are inverted by transmitter side or not. The DBI shall be synchronized with DQ signals. DBI is regarded as DQ, such that specifications such as AC parameters and Interface training shall be applied to DBI.

4.6.2. DBI Signal Encoding

DBI signal shall be either 0 or 1 during data input/output, where 0 indicates the DQ signals in the same cycle are not inverted and 1 indicates the DQ signals in the same cycle are inverted.
In the case where transmitter (host or NAND device) outputs DQ with DBI, the transmitter shall invert DQ signal on the pin and set DBI to 1 if the number of 1's of internal DQ signals is more than 4. Otherwise, if the number of 1's is equal to or less than 4, the transmitter shall not invert DQ signal on the pin and set DBI to 0.

DBI function shall be activated/deactivated by Set Feature.

The table below shows the DQ bus and DBI signal behavior during different modes of operation:

Mode of Operation	DQ[7:0] Behavior	DBI signal Behavior
Command/address	Without DBI encoding	"0"
Data Input	With DBI encoding	Encoding flag
Data Output	With DBI encoding	Encoding flag
SET Feature / GET Feature / Read ID / Read Status	Without DBI encoding	"0"
Write DQ Training (Tx side)	Without DBI encoding	9th DQ
Read DQ Training	Without DBI encoding	9th DQ (inverse mask value "0")

Table 4-4 DQ bus and DBI signal behavior

4.7. Test Conditions

4.7.1. Test Conditions for Timing

The test conditions that shall be used to verify compliance with a particular timing mode for devices are listed in the table below. The test conditions are the same regardless of the number of LUNs per Target.

Parameter	NV-LPDDR4 (LTT)	NV-LPDDR4 with VccQL (PI-LTT)
Positive input transition	VIL.LTT (DC) to VIH.LTT (AC)	VIL.PI-LTT (DC) to VIH.PI-LTT (AC)
Negative input transition	VIH.LTT (DC) to VIL.LTT (AC)	VIH.PI-LTT (DC) to VIL.PI-LTT (AC)
Minimum input slew rate (only for DQS_x_t/c and RE_x_n/c [1])	~~1.0 V/ns (for single-ended signals), 2.0 V/ns (for differential signals)~~ 1V/ns to 7V/ns for ≤ 3.6GT/s 1.5V/ns to 7V/ns for >3.6GT/s	~~1.0 V/ns (for single-ended signals), 2.0 V/ns (for differential signals)~~ 1V/ns to 7V/ns for ≤ 3.6GT/s 1.5V/ns to 7V/ns for >3.6GT/s
Input timing levels	Crosspoint	Crosspoint
Output timing levels	Crosspoint	Crosspoint
Output Driver strength	Default[1]	Default[2]

NOTE:
1) Input slew rate is only valid for strobe signals such as DQS_x_t/c and RE_x_n/c, not for DQ. These are single-ended specifications for each signal in the differential pair.
2) Default value is 37.5 Ohms for the pull-down setting, and 50 Ohms Channel ODT or less (VSP) setting for the pull-up

Table 4-5 Testing Conditions for Timing Specs

4.7.2. Output Timings Reference Loads

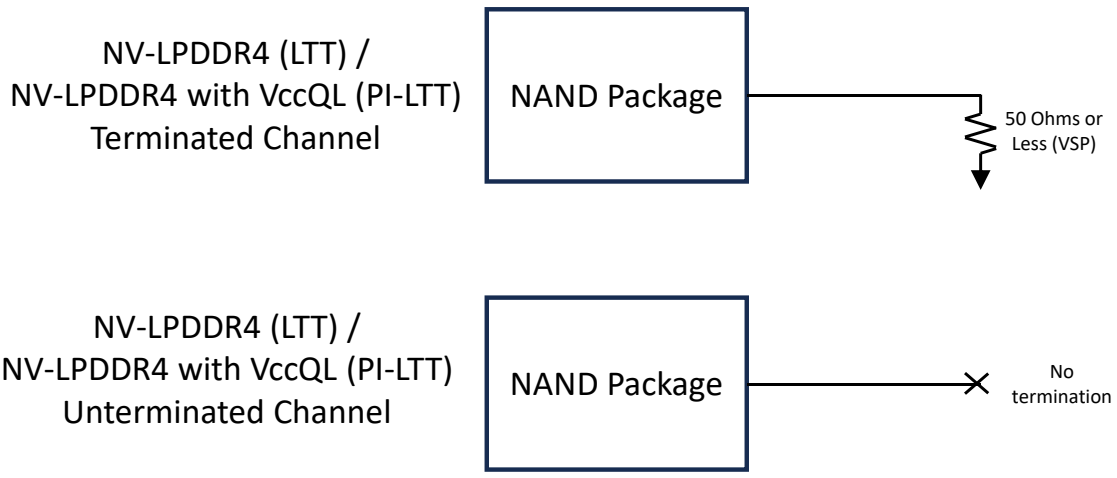


Figure 4-6 Output Timing Reference Loads for Timing Specs

The “Output Timing Reference Loads” are not intended as a precise representation of any particular system environment, or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to their system environment.

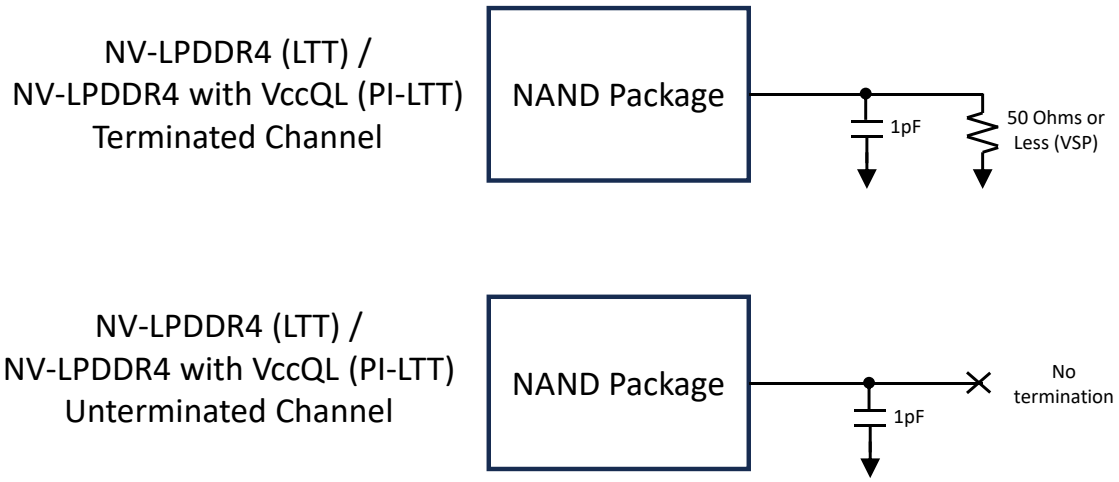


Figure 4-7 Output Timing Reference Loads for Output Slew Rate

4.7.3. Output Slew Rate

The output slew rate requirements that the device shall comply with are defined in the table below.

Description	Output Slew Rate		Unit
	Min	Max	
Single Ended	1	5.0	V/ns
Differential	2	10.0	V/ns

Table 4-6 Output Slew Rate Requirements for NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) with ZQ calibration

The testing conditions that shall be used to verify the output slew rate are listed in the table below. Output slew rates are only verified with ZQ calibration enabled.Output slew rate is verified by design and characterization; it may not be subject to production test.

The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate. Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal. The differential parameters are used when the DQS signal is configured to operate as a differential signal.

Parameter	NV-LPDDR4 (LTT)	NV-LPDDR4 with VccQL (PI-LTT)
VOL(DC)	—	—
VOH(DC)	—	—
VOL(AC)	0.2 * VOH.LTT,nom	0.2 * VOH.PI-LTT,nom
VOH(AC)	0.8 * VOH.LTT,nom	0.8 * VOH.PI-LTT,nom
VOLdiff(AC)	-0.6 * VOH.LTT,nom	-0.6 * VOH.PI-LTT,nom
VOHdiff(AC)	0.6 * VOH.LTT,nom	0.6 * VOH.PI-LTT,nom
Positive output transition	VOL (AC) to VOH (AC) VOLdiff(AC) to VOHdiff(AC)	VOL (AC) to VOH (AC) VOLdiff(AC) to VOHdiff(AC)
Negative output transition	VOH (AC) to VOL (AC) VOHdiff(AC) to VOLdiff(AC)	VOH (AC) to VOL (AC) VOHdiff(AC) to VOLdiff(AC)
tRISE[1]	Time during rising edge from VOL(AC) to VOH(AC)	Time during rising edge from VOL(AC) to VOH(AC)
tFALL[1]	Time during falling edge from VOH(AC) to VOL(AC)	Time during falling edge from VOH(AC) to VOL(AC)
tRISEdiff[2]	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)	Time during rising edge from VOLdiff(AC) to VOHdiff(AC)
tFALLdiff[2]	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)	Time during falling edge from VOHdiff(AC) to VOLdiff(AC)
Output slew rate rising edge	[VOH(AC) – VOL(AC)] / tRISE [VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff	[VOH(AC) – VOL(AC)] / tRISE [VOHdiff(AC) – VOLdiff(AC)] / tRISEdiff
Output slew rate falling edge	[VOH(AC) – VOL(AC)] / tFALL [VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff	[VOH(AC) – VOL(AC)] / tFALL [VOHdiff(AC) – VOLdiff(AC)] / tFALLdiff
Output reference load	1pF to Vss	1pF to Vss

NOTE:
1. Refer to Figure 4-8.
2. Refer to Figure 4-9.

Table 4-7 Testing Conditions for Output Slew Rate

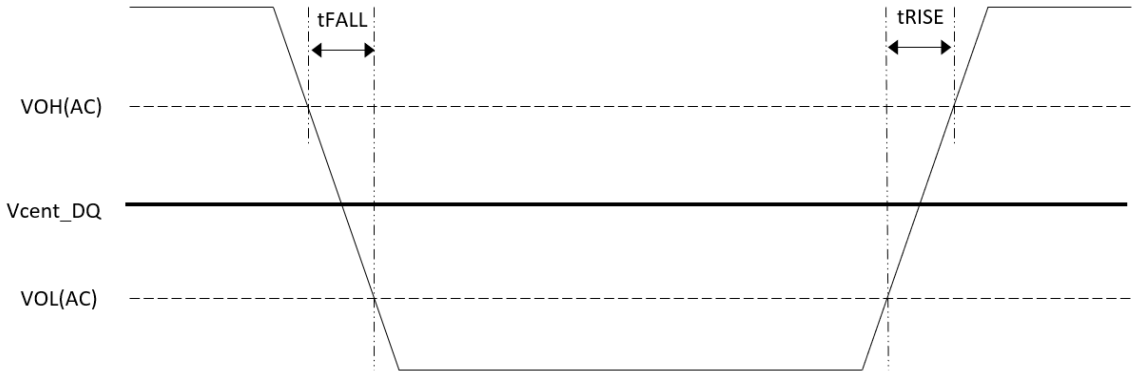


Figure 4-8 tRISE and tFALL Definition for Output Slew Rate (single-ended)

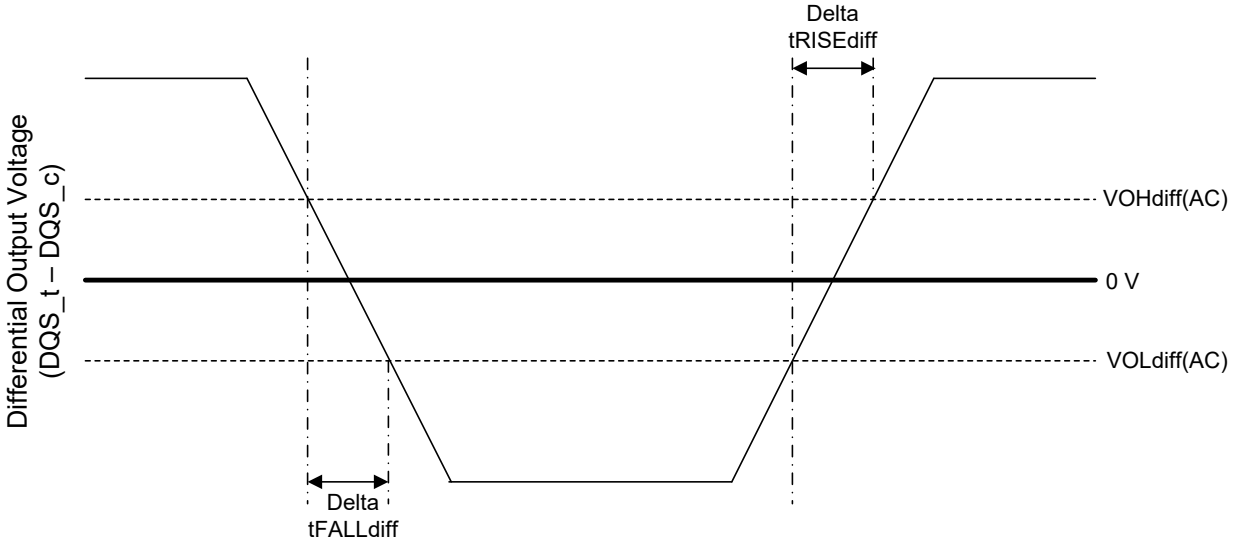


Figure 4-9 tRISEdiff and tFALLdiff Definition for Output Slew Rate (differential)

The output slew rate matching ratio is specified in the table below. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling is faster than the rising edge, then divide the falling slew rate by the rising slew rate. The output slew rate mismatch is verified by design and characterization; it may not be subject to production test

Parameter	Min	Max
Output Slew Rate Matching Ratio, without ZQ calibration	1.0	1.4
Output Slew Rate Matching Ratio, with ZQ calibration	1.0	1.3

Table 4-8 Output Slew Rate Matching Ratio

4.8. ZQ Calibration

ZQ calibration is required for both the NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces regardless of data rate.

ZQ Calibration is performed by issuing F9h command for ZQCL (ZQ long calibration) and D9h command for ZQCS (ZQ short calibration). ZQ Calibration is used to calibrate NAND Ron values and may also be used to calibrate ODT values as well. A longer time is required to calibrate the output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL is used to perform the initial calibration after power-up initialization sequence. The command to enable ZQCL may be issued at any time by the controller depending on the system environment. ZQCL triggers the calibration engine inside the NAND and once calibration is achieved, the calibrated values are transferred from the calibration engine to NAND IO, which updates the output driver and on-die termination values.

ZQCL is allowed a timing period of tZQCL to perform the full calibration and the transfer of values.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 1.5 % (ZQ Correction) of R_{ON} and Rtt impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in 4.9.3 Output Driver Sensitivity and 4.13.1 ODT Sensitivity sections. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the NAND is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$ZQCorrection / [(TSens\ X\ Tdriftrate) + (VSens\ X\ Vdriftrate)]$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the NAND temperature and voltage sensitivities.

For example, if TSens = 0.5% / oC, VSens = 0.2% / mV, Tdriftrate = 1 oC / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$1.5/\ [(0.5\ X\ 1) + (0.2\ X\ 15)] = 0.429 = 429ms$$

No other activities, including read status, should be performed on the NAND channel (i.e. data bus) by the controller for the duration of tZQCL or tZQCS. The quiet time on the NAND channel allows accurate calibration of output driver and on-die termination values. For multi-channel packages, all channels should not have any data transfer during ZQ calibration even if the devices are not sharing a channel with the LUN performing ZQ calibration. Once NAND

calibration is achieved, the NAND should disable ZQ current consumption path to reduce power. NAND array operations may not occur on the device performing the ZQCS or ZQCL operation. NAND array operations may occur on any devices that share the ZQ resistor with the device performing ZQCS or ZQCL. All devices connected to the DQ bus shall be in high impedance during the calibration procedure. The R/B# signal will be brought low by the device during calibration time, but if other devices are driving a shared R/B# low then the host is required to wait the maximum tWB+tZQCS before issuing any commands to the data bus.

If a RESET command is issued during ZQ calibration, the state of the NAND device output driver strength and ODT is not guaranteed and the host shall re-run calibration operation. If a RESET command (FFh, FAh, FCh) is issued during ZQ long calibration (ZQCL) operation, the RESET operation is executed and the NAND device will revert to factory settings for output driver strength and ODT values (e.g. as if no ZQ calibration was performed). If a RESET command (FFh, FAh, FCh) is issued during ZQ short calibration (ZQCS) operation, the RESET operation is executed and the NAND device will return to vendor specific settings for output driver strength and ODT values. When either ZQCL or ZQCS is aborted with a RESET command, the reset time will be less than 10us (i.e. tRST < 10us).

In systems that share the ZQ resistor between NAND devices, the controller must not allow any overlap of tZQCL or tZQCS between the devices.

4.8.1. ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ Calibration function, a RZQ = 300 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The ZQ resistance is the sum of the trace resistance and the actual resistor resistance. The user should attempt to place ZQ resistor as close as possible to the NAND device to reduce the trace resistance. The resistance presented to the NAND needs to be +/-1% of 300 Ohm. The vendor may require a limit to the number of LUNs (and channels) a single RZQ resistor can be shared amongst. A single resistor can be used for each NAND device or one resistor can be shared between up to the vendor specified number of NAND devices if the ZQ calibration timings for each NAND do not overlap. The Cdie component of the ZQ signal will be less than an I/O signal. Depending on the number of die per package the total capacitance (Cpackage + Cdie) of the ZQ signal may exceed an I/O signal. For packages with eight or more die that share a ZQ signal the total ZQ capacitance will not exceed 15% greater than the number of die times the Cdie of an I/O signal [i.e. Total ZQ capacitance < 1.15 * Cdie(I/O)].

4.9. Output Specifications

A device may be configured to a different output driver strength via the Set Features (EFh) or Set Features by LUN (D5h) command.

4.9.1. Output Pull-Down Drive Strengths

Setting	NV-LPDDR4 (LTT)	NV-LPDDR4 with VccQL (PI-LTT)
25 Ohms	RZQ/12	Not supported
37.5 Ohms[1,3]	RZQ/8	RZQ/8
42.9 Ohms	RZQ/7	RZQ/7
50 Ohms[1,3]	RZQ/6	RZQ/6
60 Ohms	RZQ/5	RZQ/5
75 Ohms	RZQ/4	RZQ/4
100 Ohms	RZQ/3	RZQ/3
150 Ohms	RZQ/2	RZQ/2

NOTE:
1. 37.5Ω and 50Ω Pull-Down drive strengths are mandatory while the rest are vendor specific.
2. With ZQ Calibration, Pull-Down tolerance from the nominal value is ±15% (when measured at a pad voltage of VOH_nom)
3. The default value when Pull-Down bit locations are in Feature Address 22h is 50Ω while the default value when Pull-Down bit locations are in Feature Address 10h is 37.5Ω.

Table 4-9 Output Pull-Down Drive Strength Settings for NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT)

4.9.2. Output Pull-Up VOH,nom Values

The values for NV-LPDDR4 (LTT) data interface VOH with ZQ calibration are specified in the table below:

Description	VOH.LTT setting	VOH.LTT Maximum	VOH.LTT,nom @ 1.2V VCCQ	VOH.LTT Minimum	Unit
R_pullup	VCCQ/3	1.15 * VOH.LTT,nom	400	0.85 * VOH.LTT,nom	mV
R_pullup	VCCQ/2.5	1.15 * VOH.LTT,nom	480	0.85 * VOH.LTT,nom	mV

Notes:
1. VOH.LTT,nom = VccQ/3 is mandatory and shall be the default, while VOH.LTT,nom = VccQ/2.5 is optional.
2. VOH accuracy requirements are after ZQ calibration with an RZQ of 300Ω +/- 1%
3. VOH accuracy requirements only apply at valid CH_ODT values
4. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

Table 4-10 VOH Values for NV-LPDDR4 (LTT) with ZQ calibration

The values for NV-LPDDR4 with VccQL (PI-LTT) data interface VOH with ZQ calibration are specified in the table below:

Description	VOH. PI-LTT setting	VOH.PI-LTT Maximum	VOH.PI-LTT,nom @ 0.6V VccQL	VOH.PI-LTT Minimum	Unit
R_pullup	VccQL/2	1.15 * VOH.PI-LTTnom	300	0.85 * VOH.PI-LTTnom	mV

Notes:
1. VOH.PI-LTT,nom = VccQL/2 is mandatory and shall be the default
2. VOH accuracy requirements are after ZQ calibration with an RZQ of 300Ω +/- 1%
3. VOH accuracy requirements only apply at valid CH_ODT values
4. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.

Table 4-11 VOH Values for NV-LPDDR4 with VccQL (PI-LTT) with ZQ calibration

Channel ODT Setting	Unit	NV-LPDDR4 (LTT)		NV-LPDDR4 with VccQL (PI-LTT)
		VOH.LTT Nominal = VCCQ/3	VOH.LTT Nominal = VCCQ/2.5	VOH.PI-LTT Nominal = VCCQL/2
25 Ohms	RZQ/12	Valid	Valid	Invalid
37.5 Ohms	RZQ/8	Valid	Valid	Valid
42.9 Ohms	RZQ/7	Valid	Valid	Valid
50 Ohms	RZQ/6	Valid [1] (default)	Valid [2]	Valid [3] (default)
60 Ohms	RZQ/5	Valid	Valid	Valid
75 Ohms	RZQ/4	Valid	Valid	Valid
100 Ohms	RZQ/3	Valid	Valid	Valid
150 Ohms	RZQ/2	Valid	Valid	Valid

NOTE:
1. Support for Pull-Up Setting with a Channel ODT value of 50Ω when VOHpu,nom = VccQ/3 is mandatory and shall be the default setting. Support for other values is vendor specific.
2. Support for VOH.LTT.nom = VccQ/2.5 is optional. When VOH.LTT,nom = VccQ/2.5 is supported by a device the CH_ODT configurations that are supported as well as the default value are vendor specific.
3. Support for CH_ODT value of 50Ω when VOH.PI-LTT,nom = VccQL/2 is mandatory and shall be the default setting. Support for other CH_ODT values is vendor specific.

Table 4-12 Allowable I/O Pull-Up Settings (CH_ODT) for NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT)

4.9.3. Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits can be expected to widen according to the tables bellow:

Description	VOUT to VssQ	Maximum	Minimum	Unit
R_pullup for LTT	VOH.LTT,nom	1.15 + dVOHdT x ΔT + dVOHdV x ΔV	0.85 - dVOHdT x ΔT - dVOHdV x ΔV	%
R_pullup for PI-LTT	VOH.PI-LTT,nom	1.15 + dVOHdT x ΔT + dVOHdV x ΔV	0.85 - dVOHdT x ΔT - dVOHdV x ΔV	%

Table 4-13 Output Driver Sensitivity Definition

Change	Maximum	Minimum	Unit
dRONdT	0.5	0	%/°C
dRONdV	0.2	0	%/mV
dVOHdT	0.5	0	%/°C
dVOHdV	0.2	0	%/mV

Table 4-14 Output Driver Voltage and Temperature Sensitivity

4.10. Capacitance

4.10.1. Package Electrical Specifications for DQS_t, DQS_c, DQ[7:0], RE_t, RE_c, DBI

ZIO applies to DQ[7:0], DQS_t, DQS_c, RE_t, RE_c and DBI. TdIO RE applies to RE_t and RE_c. TdIO and TdIOMismatch applies to DQ[7:0], DQS_t, DQS_c and DBI. Mismatch and Delta values are required to be met across same data bus on given package (i.e. package channel), but not required across all channels on a given package.

Symbol	Parameter	≤400 MT/s		533 MT/s		667 MT/s		800 MT/s to 1200 MT/s		1333 MT/s to 3600 MT/s		3600 MT/s to 4800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Z_{IO}	Input/Output Zpkg	35	90	35	90	35	90	35	90	35	90	30	80	Ohms
Td_{IO}	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	-	130	-	115	ps
$Td_{IO\ RE}$	Input/Output Pkg Delay	-	160	-	160	-	145	-	130	-	130	-	115	ps
Td_{IO}Mismatch	Input/Output Pkg Delay Mismatch	-	50	-	40	-	40	-	40	-	40	-	40	ps
D $Z_{IO\ DQS}$	Delta Zpkg for DQS_t and DQS_c	-	10	-	10	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ DQS}$	Delta Pkg Delay for DQS_t and DQS_c	-	10	-	10	-	10	-	10	-	10	-	10	ps
D $Z_{IO\ RE}$	Delta Zpkg for RE_t and RE_c	-	10	-	10	-	10	-	10	-	10	-	10	Ohms
D $Td_{IO\ RE}$	Delta Pkg Delay for RE_t and RE_c	-	10	-	10	-	10	-	10	-	10	-	10	ps

NOTE:

1. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with Vcc, VccQ/VccQL, Vss, VssQ shorted with all other signal pins floating. The inductance is measured with Vcc, VccQ/VccQL, Vss and VssQ shorted and all other signal pins shorted at the die side (not pin).
2. Package only impedance (Z_{IO}) is calculated based on the Lpkg and Cpkg total for a given pin where: Z_{IO}(total per pin) = SQRT(Lpkg/Cpkg)
3. Package only delay (Td_{IO}) is calculated based on Lpkg and Cpkg total for a given pin where: Td_{IO}(total per pin) = SQRT(Lpkg*Cpkg)
4. Mismatch for Td_{IO} (Td_{IO}Mismatch) is value of Pkg Delay of fastest I/O minus the value of Pkg Delay for slowest I/O.
5. Delta for DQS is Absolute value of ZIO(DQS_t-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO (DQS_t)-TdIO(DQS_c) for delay(Td)
6. Delta for RE is Absolute value of ZIO(RE_t-ZIO(RE_c) for impedance(Z) or absolute value of TdIO(RE_t)-TdIO(RE_c) for delay(Td)

Table 4-15 Package Electrical Specifications

4.10.2. Pad Capacitance Specifications for DQS_t, DQS_c, DQ[7:0], RE_t, RE_c, DBI and ZQ Pins

Symbol	Parameter	≤1200 MT/s		1200 MT/s to 2400 MT/s		2400 MT/s to 3600 MT/s		3600 MT/s to 4800 MT/s		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
C_{IO}	Input/Output Capacitance for DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, DBI	-	2.5	-	1.6	-	1.6	-	1.2	pF
C_{ZQ}	ZQ capacitance	-	2.875	-	2.875	-	2.875	-	2.875	pF
$D C_{IO}$ DQS	Delta Input/Output Capacitance DQS_t and DQS_c	0	0.2	0	0.2	0	0.2	0	0.2	pF
$D C_{IO}$ RE	Delta Input/Output Capacitance for RE_t and RE_c	0	0.2	0	0.2	0	0.2	0	0.2	pF

NOTE:

1. These parameters are not subject to a production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with Vcc, VccQ, VccQL, Vss, and VssQ applied and all other pins floating (accept the pin under test). VccQ = VccQL = 1.2V, VBIAS = 0.2V and on-die termination off for NV-LPDDR4 (LTT) interface. VccQ = 1.2V, VccQL = 0.6V, VBIAS = 0.15V and on-die termination off for NV-LPDDR4 with VccQL (PI-LTT) interface.
2. These parameters apply to monolithic die, obtained by de-embedding the package L & C parasitics.
3. Delta for DQS is the absolute value of CIO(DQS_t) - CIO(DQS_c)
4. Delta for RE is the absolute value of CIO(RE_t) - CIO(RE_c)

Table 4-16 Pad Capacitance for DQS_t, DQS_c, DQ[7:0], RE_t, RE_c, DBI and ZQ Pins

4.10.3. Input Capacitance Specifications for ALE, CE_n, CLE, WE_n and WP_n

The input capacitance requirements defined in table below is for packaged raw NAND devices. The testing conditions that shall be used to verify the input capacitance requirements are: temperature of 25 degrees Celsius, VccQ = nominal value, Vcc = nominal value, V_{IN} = 0v, and a frequency of 100 MHz. The DC_{IN} specification is for the ALE, CLE and WE_n pins only and is the maximum variation allowed for those pins as a group.

Parameter	Loading	Min	Typ	Max	Unit
C_{IN}	1 LUN per x8 data bus	-	-	6.4	pF
	2 LUNs per x8 data bus	-	-	9.2	pF
	4 LUNs per x8 data bus	-	-	14.3	pF
	8 LUNs per x8 data bus	-	-	27.3	pF
DC_{IN} [1]	1 LUN per x8 data bus	-	-	1.4	pF
	2 LUNs per x8 data bus	-	-	1.7	pF
	4 LUNs per x8 data bus	-	-	2.0	pF
	8 LUNs per x8 data bus	-	-	4.0	pF

NOTE:
1. DC_{IN} applies to ALE, CLE and WE_n pins as a group (WE_n pin may be excluded from the group)

Table 4-17 Capacitance Specifications for ALE, CE_n, CLE, WE_n and WP_n Pins

4.11. Electrostatic Discharge Sensitivity Characteristics

Parameter[1]	Symbol	Min	Max	Unit	Notes
Human Body Model (HBM)	ESD_{HBM}	1000	-	V	2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	3
Note:1 State-of-the-art basic ESD control measures have to be in place when handling devices Note:2 Refer to ESDA / JEDEC Joint Standard JS-001 for measurement procedures Note:3 Refer to ESDA / JEDEC Joint Standard JS-002 for measurement procedures					

Table 4-18 Electrostatic Discharge Sensitivity Characteristics

4.12. Warmup Cycles

To support higher speed operations, warmup cycles for data output and/or data input may be provided. When the feature is enabled, extra cycles are initiated at the start of each data burst to improve the signal integrity of DQ/DQS/DBI/RE signals prior to the transfer of the actual user data. The intent of the extra cycles being the reduction in the number of bit errors in the user data, especially in the first few bytes of the data burst.

Warmup cycles are enabled via the Interface Configuration Register (FA 02h). When enabled for data input or data output cycles, the configured number of warmup cycles shall apply for all subsequent commands that have data input or data output cycles (including commands with SDR output), after the Set Features is complete.

Warmup cycles for data output provide extra RE_n and corresponding DQS transitions at the beginning of a data output burst. The number of extra cycles configured via the Interface Configuration includes a full data output cycle (both rising and falling edge for RE_n and DQS). When the NAND Output DFE DQ Pre-Drive feature is disabled, there is no requirement on the warmup cycles output data pattern for the DQ/DBI signals. However, when the Output DFE DQ Pre-Drive feature is enabled, there is an output data pattern requirement for DQ/DBI signals (see DFE section for more details).

Warmup cycles for data input provide extra DQS transitions at the beginning of a data input burst. The number of extra cycles configured via the Interface Configuration Register includes a full data input cycle (both rising and falling edge for DQS). When the NAND Input DFE feature is disabled,

there is no requirement on the warmup cycles input data pattern for the DQ/DBI signals. However, when the NAND Input DFE feature is enabled, there is an input data pattern requirement for DQ/DBI signals (see DFE section for more details).

Warmup cycles are optional for both data output and data input. When both are enabled, the number of warmup cycles for data output do not need to match the number of warmup cycles for data input (they do not need be configured to the same value).

The host shall take care to avoid signal integrity issues due to data burst pausing and resuming. In the Conv. Protocol, if the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. However, if the host exits the data burst by bringing ALE, CLE or CE_n high without latching with WE_n, and re-enters the data burst, warmup cycles are required for the data burst re-entry. Data burst pausing and resuming without warmup cycles is only allowed up to a certain data rate, please refer to the Pausing Data Input/Output and Restarting an Exited Data Input/Output Sequence section for more details.

The figure below shows an example of warmup cycles for data output, where the number of warmup cycles is two. In the illustration, the first byte of user data is transmitted to the host as part of the third rising transition of DQS.

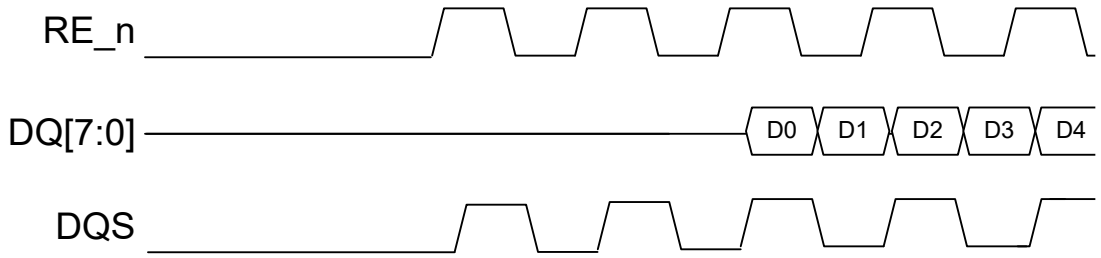


Figure 4-10 Warmup Cycles for Data Output

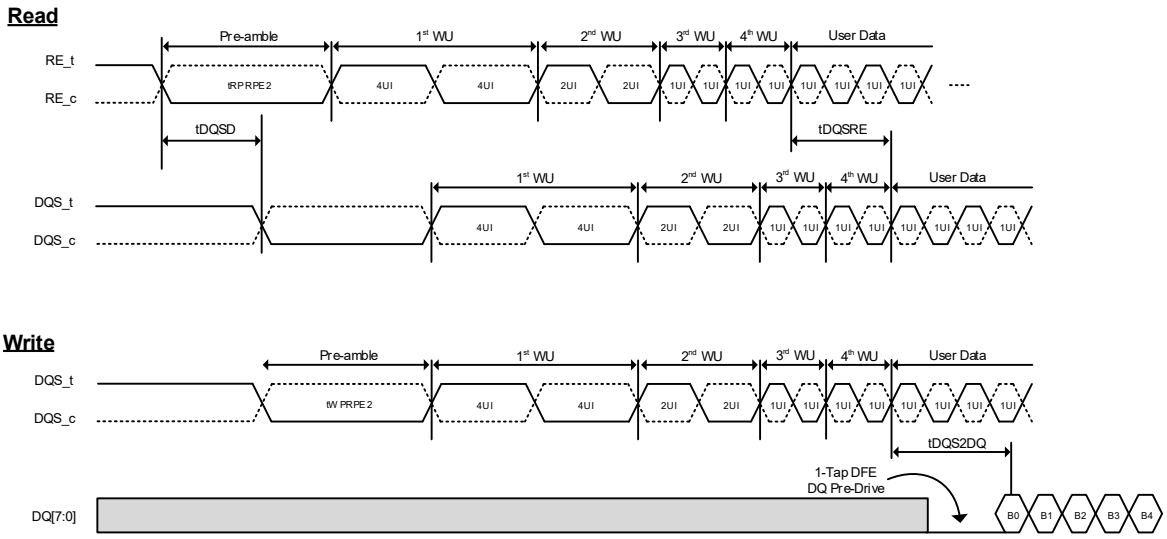
4.12.1. Progressive Warmup Cycles

As data rates increase, it becomes increasingly difficult to guarantee the correct number of differential signal toggles if the channel is not progressively warmed up.

Incorrect detection of the number of differential signal toggles can result in missing initial byte/s of data and data burst misalignment

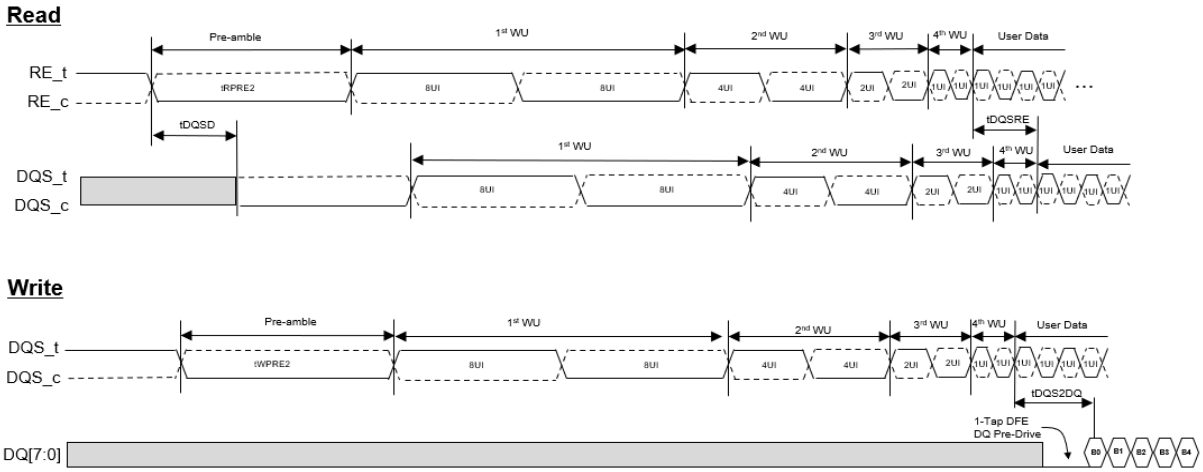
It is recommended (but optional) for the host to issue progressive warmup cycle timings at >3600MT/s.

Examples of progressive warmup cycle schemes are shown in the figures below:



NOTE: WU=Warmup Cycle

Figure 4-11 4-2-1-1 Progressive Warmup Cycle for Read/Write Example (Recommended)



NOTE: WU=Warmup Cycle

Figure 4-12 8-4-2-1 Progressive Warmup Cycle for Read/Write Example

≤ 3.6GT/s			> 3.6GT/s		
1 cycle	2 cycle	4 cycle	1 cycle	2 cycle	4 cycle
1UI	1UI x 2	1UI x 4	2UI [1)] or 1UI	2UI-1UI [1)] or 1UI x 2	4-2-1-1 UI [1)] or 8-4-2-1 UI or 1UI x 4
Note: 1) Recommended					

Table 4-19 Progressive Warmup Cycle Pattern According to Number of Warmup Cycles

4.13. On-Die Termination (ODT)

On-die termination (ODT) may be required to operate DQ[7:0], DBI, DQS_t, DQS_c, RE_t, and RE_c signals at higher speeds.

Additional power is expected to be burned from ODT. If power needs to be optimized in a particular condition, then on-die termination may be disabled, and the topology may potentially need to be run at a slower speed.

ODT settings are configured during initialization. For the Conv. Protocol, the host may configure ODT in Self-Termination configuration or the more flexible Matrix Termination configuration. For the SCA protocol, the host may configure both ODT Self-Termination and Non-Target ODT settings.

In the Conv. Protocol, both ODT Self-Termination and Matrix ODT Termination is asserted/de-asserted by the LUN based on the type of cycle (on for data input and output cycles, off for command, and address cycles). On-die termination applies for data input and output cycles for all commands. ODT is disabled when ALE, CLE or CE_n transitions from low to high.

In the Conv. protocol, for the simple configuration of self-termination only ODT, no ODT matrix configuration is required. ODT Self-Termination is configured via the Interface Configuration Register. For the more flexible Matrix Termination configuration, the host configures a matrix that defines the LUN(s) that terminate for a particular Volume. Matrix Termination enables a mixture of Target and non-Target termination to be specified This matrix is configured using the ODT Configure command. To use matrix termination for non-Target termination or termination topologies that use multiple terminators, the Volume address mechanism shall be used and the on-die termination configuration matrix shall be specified using the ODT Configure command. If using matrix termination, the ODT Configure command shall be issued to at least one LUN on all NAND Targets. As part of the ODT Configure command, Rtt settings may be specified on a per LUN basis with individual values for:

- RE_n Rtt,
- DQ[7:0], DBI and DQS for data output Rtt, and
- DQ[7:0], DBI and DQS for data input Rtt

In the SCA protocol, ODT Self-Termination is asserted/de-asserted by the LUN based on the type of bus cycle on the data bus (on during data input and output cycles), however, non-target ODT operation is controlled by NTO packets. Please refer to the Separate Commands Address (SCA) Protocol section, sub-sections 5.9.4 and 5.9.5 for more information on SCA Protocol ODT Self-Termination operation and sub-section 5.9.7 for more information on SCA Protocol Non-Target ODT (NTO) Packet operation.

Rtt	VOUT to Vss	Maximum	Nominal	Minimum	Unit
25 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/12
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
37.5 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/8
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
42.9 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/7
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
50 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/6
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
60 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/5
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
75 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/4
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
100 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/3
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
150 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/2
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	
300 Ohm	0.1 x VccQ	1.15	1.0	0.75	RZQ/1
	0.33 x VccQ [4]	1.15	1.0	0.85	
	0.5 x VccQ	1.35	1.0	0.85	

NOTE:
1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to ODT Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).
4. For VOH.LTT,nom=VccQ/2.5 setting use 0.4 x VccQ

Table 4-20 NV-LPDDR4 (LTT) Rtt effective impedances, with ZQ calibration

Rtt	VOUT to Vss	Maximum	Nominal	Minimum	Unit
37.5 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/8
42.9 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/7
50 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/6
60 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/5
75 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/4
100 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/3
150 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/2
300 Ohm	0.5 x VccQL	1.15	1.0	0.85	RZQ/1

NOTE:
1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to ODT Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

Table 4-21 NV-LPDDR4 with VccQL (PI-LTT) Rtt effective impedances, with ZQ calibration

4.13.1. ODT Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the ODT tolerance limits widen according to the table below. ODT sensitivity specifications are not tested in production but are simulated and characterized.

Description	Maximum	Minimum	Unit
Rtt for NV-LVDDR4 (LTT) [1]	1.15 + dRTTdT x ΔT + dRTTdV x ΔV	0.85 - dRTTdT x ΔT - dRTTdV x ΔV	RZQ/n
Rtt for NV-LPDDR4 with VccQL (PI-LTT) [2]	1.15 + dRTTdT x ΔT + dRTTdV x ΔV	0.85 - dRTTdT x ΔT - dRTTdV x ΔV	RZQ/n

NOTE:
1. NV-LPDDR4 (LTT) interface Rtt Maximum and Minimum specifications in this table are referenced at 0.33 x VccQ. The ODT Voltage and Temperature Sensitivity specs dRTTdT and dRTTdV are also referenced at 0.33 x VccQ.
2. NV-LPDDR4 with VccQL (PI-LTT) interface Rtt Maximum and Minimum specifications in this table are referenced at 0.5 x VccQL. The ODT Voltage and Temperature Sensitivity specs dRTTdT and dRTTdV are also referenced at 0.5 x VccQL.

Table 4-22 ODT Sensitivity Definition

Change	Maximum	Minimum	Unit
dRTTdT	0.5	0	%/°C
dRTTdV	0.2	0	%/mV

Table 4-23 ODT Voltage and Temperature Sensitivity

4.13.2. Self-termination ODT

When self-termination is enabled, the LUN that is executing the command provides on-die termination. Self-termination ODT is enabled using Set Features to the Interface Configuration Register (FA02h). Self-termination ODT is supported on both the Conv. and SCA protocols.

The figure below defines Conv. Protocol self-termination only ODT enable and disable requirements for the LUN that is the executing the command when self-termination ODT is enabled. If the ODT Configure command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to Matrix Termination.

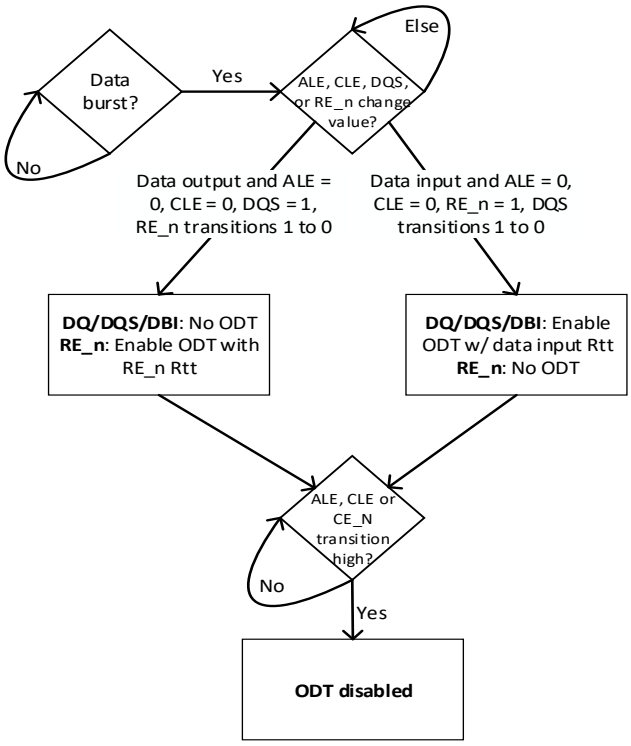


Figure 4-13 Conv. Protocol Self-Termination ODT Behavioral Flow

The figure below shows the SCA Protocol Self-Termination ODT Behavioral Flow for the LUN that is the executing the data burst when self-termination ODT is enabled on the LUN:

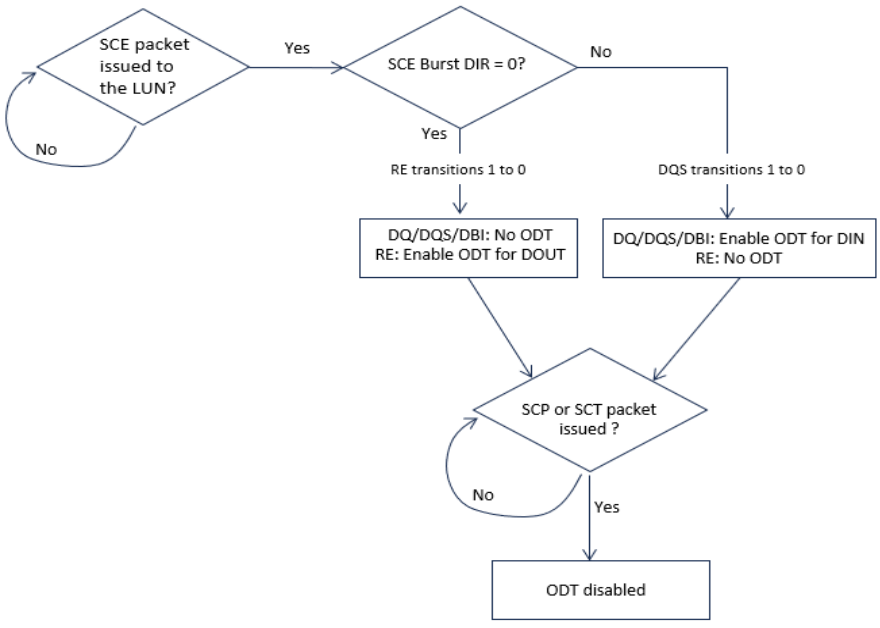


Figure 4-14 SCA Protocol Self-Termination ODT Behavioral Flow

4.13.3. Matrix Termination (Conv. Protocol Only)

A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT Configure command) may be located on the same Volume as the Volume it is terminating for (Target termination) or a separate Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in the table below.

LUN is on Selected Volume ?	Terminator for Selected Volume ?	LUN State	ODT Actions Defined
Yes	na	Selected	Figure 4-15
No	Yes	Sniff	Figure 4-16
No	No	Deselected	No ODT actions

Table 4-24 LUN State for Matrix Termination

The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. The table below defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE_n signals.

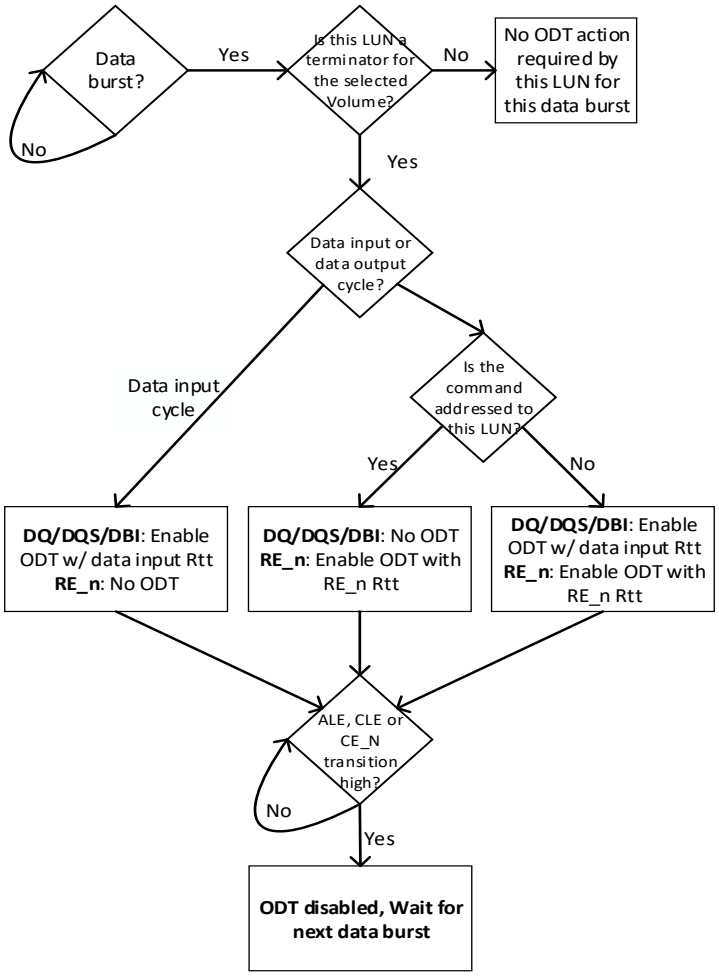


Figure 4-15 ODT Actions for LUNs on Selected Volume

The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE_n signals to determine when to enable or disable ODT. The figure below defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

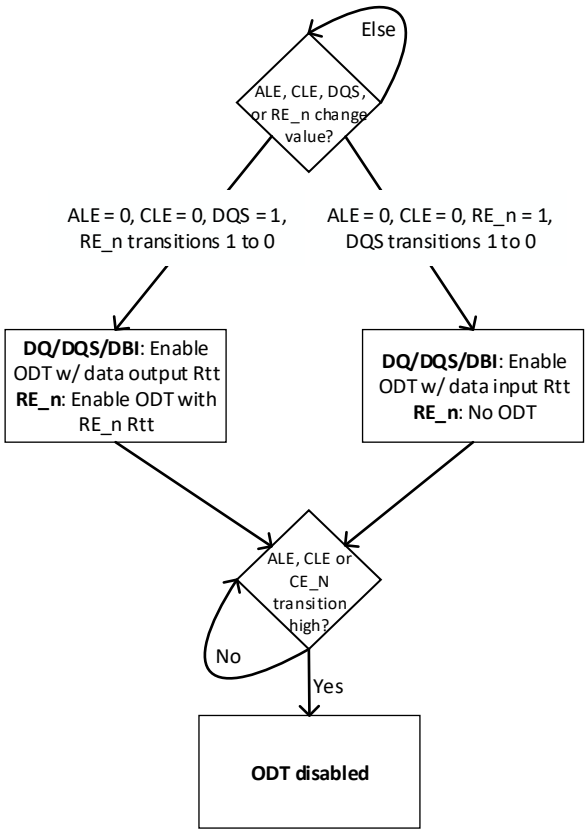


Figure 4-16 ODT Actions for LUNs in Sniff State on Unselected Volume

4.13.3.1. Matrix Termination Examples (Informative)

This section describes two examples of on-die termination configurations using matrix termination. In both examples, each Volume consists of two LUNs, referred to as H0N*n*-LUN0 and H0N*n*-LUN1. The following Volume addresses were appointed at initialization.

Volume	Appointed Volume Address
H0N0	0
H0N1	1
H0N2	2
H0N3	3

Table 4-25 Matrix Termination Example: Appointed Volume Addresses

For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination Rtt values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first

example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Refer to the ODT Configure Definition section for definition of the ODT Configuration Matrix bits (i.e. M0, M1, Rtt1, Rtt2) used in the Matrix Termination examples in this section.

LUN	M0	M1	Rtt1	Rtt2	Notes
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	01h	00h	02h	03h	Terminates for Volume 0 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N1-LUN0	02h	00h	02h	03h	Terminates for Volume 1 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N1-LUN1	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN0	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN1	04h	00h	02h	03h	Terminates for Volume 2 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N3-LUN0	08h	00h	02h	03h	Terminates for Volume 3 (Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE_n (RE_t/RE_c).
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an Rtt value 50 Ohms for DQ[7:0]/DQS.

Table 4-26 Matrix Termination Example 1

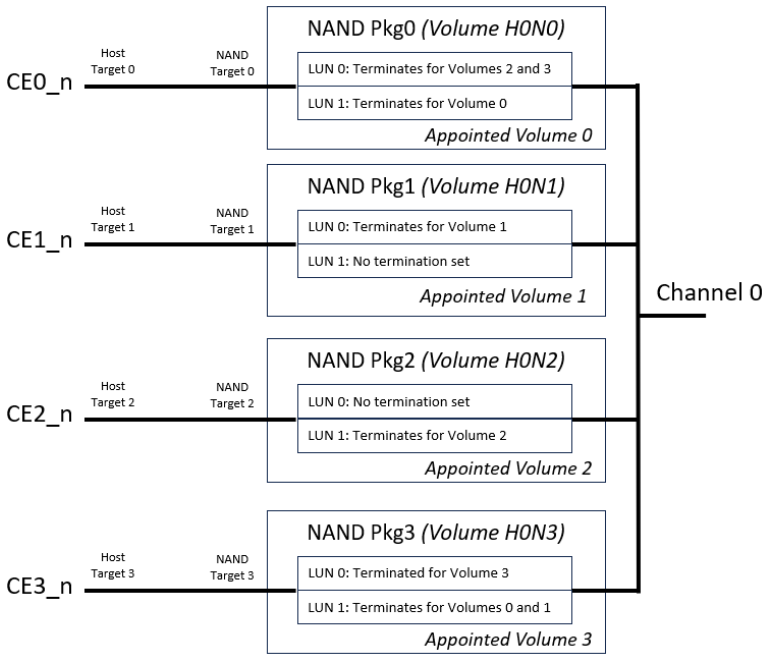


Figure 4-17 Example: Non-Target ODT for Data Output, Target ODT for Data Input

The second example uses parallel non-Target termination to achieve a stronger effective Rtt value for both data output and data input operations. For data output, two 50 Ohm terminators are used in parallel to achieve an effective 25 Ohms non-Target termination value. For data input, two 100 Ohm terminators are used in parallel to achieve an effective 50 Ohms non-Target termination value. This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate Rtt values with the use of different Rtt values for parallel LUNs. For example, if one terminator was configured for 75 Ohms and another terminator was configured for 100 Ohms for the same Volume then an effective Rtt value of 43 Ohms is achieved. In this example, parallel termination is used for data input and data output for DQ[7:0]/DQS, however, RE_n (RE_t/RE_c) is non-Target terminated with 100 Ohms using a single LUN.

LUN	M0	M1	Rtt1	Rtt2	Notes
H0N0-LUN0	0Ch	00h	42h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	0Ch	00h	42h	01h	Terminates for Volumes 2 and 3 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) with an Rtt value of 150 Ohms for RE_n (RE_t/RE_c).
H0N1-LUN0	00h	00h	00h	00h	Does not act as a terminator.
H0N1-LUN1	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN0	00h	00h	00h	00h	Does not act as a terminator.
H0N2-LUN1	00h	00h	00h	00h	Does not act as a terminator.
H0N3-LUN0	03h	00h	42h	01h	Terminates for Volumes 0 and 1 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) with an Rtt value of 150 Ohms for RE_n (RE_t/RE_c).
H0N3-LUN1	03h	00h	42h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an Rtt value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an Rtt value of 100 Ohms for DQ[7:0]/DQS.

Table 4-27 Matrix Termination Example 2

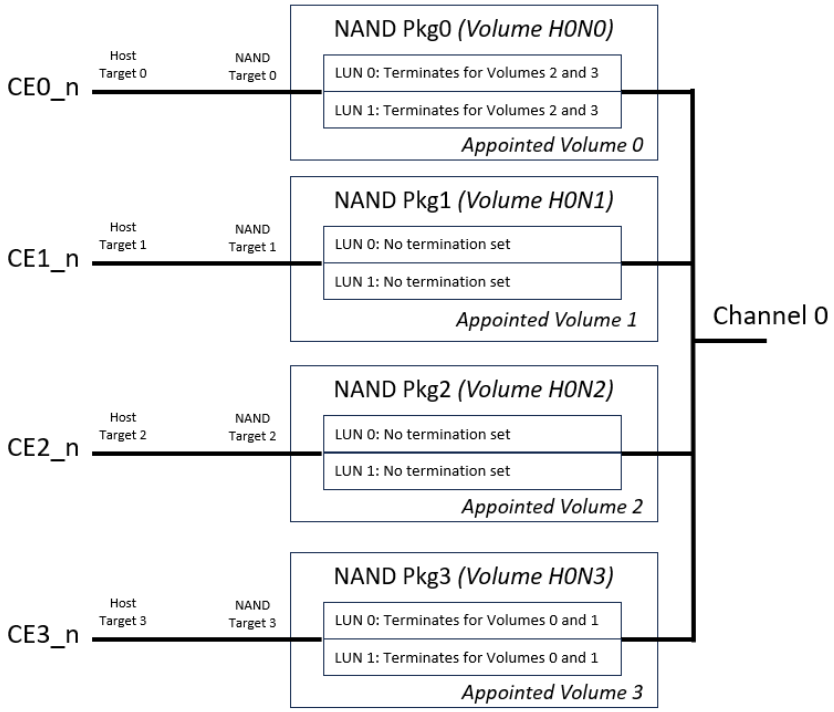


Figure 4-18 Example: Parallel Non-Target ODT

4.14. Timing Parameter Descriptions

The behavior of the device when the required minimum and maximum times are not adhered to is undefined. Note that the host needs to account for channel effects in meeting the specified timings with the device.

4.14.1. General Timing Parameters

Parameter	Description	Applicability	
		Conv. Protocol	SCA Protocol[10]
tADL[2]	Address cycle to data loading time.	Yes	Yes, though in some instances, tADL is replaced by tCDL. Also tADL value is relaxed to versus Conv. Protocol.
tCAH	Command/address DQ hold time.	Yes	No
tCALH	CLE and ALE hold time.	Yes	No, replaced by tCACH in SCA protocol.
tCALS	CLE and ALE setup time during command and address cycles.	Yes	No, replaced by tCACS in SCA protocol.
tCALQS2	CLE and ALE setup time to DQS_t or DQS_t/DQS_c cross-point.	Yes	No
tCALR2	CLE and ALE setup time to RE_n or RE_t/RE_c cross-point.	Yes	No
tCAS	Command/address DQ setup time.	Yes	No
tCCS[2,6,7]	Change Column setup time.	Yes	No, tCCS is replaced by tCCSR and tCCSW in SCA protocol.
tCEH	CE_n high hold time.	Yes	No, replaced by tCEH2 in SCA protocol.
tCH	CE_n hold time.	Yes	No, replaced by tCLKCE in SCA protocol.
tCHZ[9]	CE_n high to output Hi-Z	Yes	No
tCLHZ[9]	CLE high to output Hi-Z	Yes	No
tCLR	CLE to (RE_n low or RE_t/RE_c crosspoint).	Yes	No
tCR	CE_n to (RE_n low or RE_t/RE_c crosspoint).	Yes	No
tCR2	CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us.	Yes	No
tCS	CE_n setup time.	Yes	No, replaced by tCELCLK in SCA protocol.
tCS1	CE_n setup time for data burst with ODT disabled.	Yes	No
tCS2	CE_n setup time with DQS/DQ[7:0] ODT enabled.	Yes	No
tCD	CE_n setup time to DQS (DQS_t) low after CE_n has been high for greater than 1us.	Yes	No
tCSD	ALE, CLE, WE_n hold time from CE_n high.	Yes	No
tCDQSS	DQS setup time for data input start.	Yes	No, replaced by tSCDQSS in SCA protocol.
tCDQSH	DQS hold time for data input burst end.	Yes	No
tDBS	DQS (DQS_t) high and RE_n (RE_t) high setup to ALE, CLE and CE_n low during data burst.	Yes	No
tFEAT[1]	Busy time for Set Features, Set Features by LUN, Get Features and Get Features by LUN.	Yes	Yes

tODTOFF	ODT Disable command to next command.	Yes	No
tODTON	ODT Enable command to next command.	Yes	No
tRHW	Data output cycle to command or address cycle (RE_t high to WE_n high).	Yes	No
tRR	Ready time to data output.	Yes	No
tRST[8]	Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	Yes	Yes
tWB[3,4]	Last command or address cycle to device busy (SR[6] low).	Yes	Yes
tWC	Write cycle time.	Yes	No, replaced by tCACI spec in SCA protocol.
tWH	WE_n high pulse width,	Yes	No, replaced by tCAHPI spec in SCA protocol.
tWHR[2]	Last command or address cycle to data output.	Yes	Yes
tWHRT[5]	Last address cycle to data output for training.	Yes	Yes
tWTRN[1,5]	Busy time during Write RX Training.	Yes	Yes
tWP	WE_n low pulse width.	Yes	No, replaced by tCALPI spe in SCA protocol.
tWW	WP_n transition to command cycle.	Yes	Yes

NOTE:

1. Measured from the falling edge of SR[6] to the rising edge of SR[6].
2. tADL is used for Program operations. tWHR is used for Read ID, Read Status, and Read Status Enhanced commands. tCCS is used for commands that modify the column address and thus impact the data pipeline; these commands include Change Read Column and Change Write Column.
3. In the Conv. Protocol, for Set Features, tWB starts on the falling edge of DQS for parameter P4, whereas in the SCA Protocol, tWB starts on the last falling edge of CA_CLK for parameter P4.
4. Commands (including Read Status / Read Status Enhanced) shall not be issued until after tWB is complete.
5. tWHRT, tWTRN are used only for training commands.
6. In the Conv. Protocol, during data input sequences which require tCCS, tCCS is referenced from WE# high to:
    a. The first byte (DQS_t rising edge) input when warmup cycles are disabled.
    b. The first byte (DQS_t rising edge) of the first input warmup cycle when warmup cycles are enabled.

    See SCA section for tCCSW timing references.
7. In the Conv. Protocol, during data output sequences which require tCCS, tCCS is referenced from WE# high to the RE_t falling edge marking the start of the read pre-amble (tRPRE/tRPRE2). See SCA section for tCCSR timing references.
8. The target is allowed a longer maximum reset time when a program or erase operation is in progress. For reset time during operations other than erase, program or page read (00-address-30h) operation, refer to the vendor datasheet.
9. Refer to Appendix for measurement technique.
10. This table does not list all general interface timing parameters for the SCA protocol. See SCA Protocol section for other general interface timing parameters.

Table 4-28 General Interface Timing Parameters

Array timing parameter values are defined in the table below, please see vendor datasheet for values. These parameters apply to both Conv. and SCA protocols.

Parameter	Description
tBERS[1]	Block erase time
tPLEBSY[1, 2]	Busy time for multi-plane erase operation
tPLPBSY[1, 2]	Busy time for multi-plane program operation
tPLRBSY[1, 2]	Busy time for multi-plane read operation
tPCBSY[1]	Program cache busy time
tPROG[1]	Page program time
tR[1]	Page read time
tRCBSY[1]	Read cache busy time

NOTE:
1. Measured from the falling edge of SR[6] to the rising edge of SR[6].
2. NAND vendors may remove tPLEBSY, tPLPBSY and tPLRBSY busy times, keeping SR[6] HIGH between multi-plane sequences, and instead require the host to provide a vendor specific fixed delay between multi-plane sequences (see vendor datasheet).

Table 4-29 Array Timing Parameter Descriptions

The table below shows busy times associated with cache operations (tRCBSY, tPCBSY) and multi-plane operations (tPLEBSY, tPLPBSY, and tPLRBSY). These parameters apply to both Conv. and SCA protocols.

Parameter	Typical	Maximum
tPLEBSY [2]	500 ns	tBERS
tPLPBSY [2]	500 ns	tPROG
tPLRBSY [2]	500 ns	tR
tPCBSY	3 µs	tPROG
tRCBSY	3 µs	tR

NOTE:
1. Typical times for tPCBSY and tRCBSY are the recommended interval at which the host should consider polling status. Device busy time may be longer than the typical value.
2. NAND vendors may remove tPLEBSY, tPLPBSY and tPLRBSY busy times, keeping SR[6] HIGH between multi-plane sequences, and instead require the host to provide a vendor specific fixed delay between multi-plane sequences (see vendor datasheet).

Table 4-30 Cache and Multi-plane Short Busy Times

The table below shows timing specs associated with the Volume Select sequence. Since Volume Select is only used in Conv. Protocol, these timings do not apply to the SCA Protocol.

Parameter	Description	Minimum	Maximum
tVDLY	Delay prior to issuing the next command after a new Volume is selected using the Volume Select command.	50 ns	-
tCEVDLY	Delay prior to bringing CE_n high after a new Volume is selected using the Volume Select command.	50 ns	-

Table 4-31 Volume Select Times

The table below shows timing specs related to ZQ Calibration. These parameters apply to both Conv. and SCA protocols.

Parameter	Description	Maximum
tZQCL	Normal operation Long calibration time	1.2us
tZQCS	Normal operation Short calibration time	0.4us

NOTE:
1. Increased tZQCL and tZQCS values beyond minimum specified value may result when greater than 8 LUNs share a ZQ resistor

Table 4-32 ZQ Calibration Timing parameters

4.14.2. Data Burst Related Parameters

Parameter	Description	Applicability	
		Conv. Protocol	SCA Protocol [2]
dQSQ/dT	Change in tDQSQ versus temperature for a LUN. Computed by the dividing delta in tDQSQ by the operating temperature range of the device for a LUN. Spec is guaranteed by design and characterization and not tested in production.	Yes	Yes
dQSQ/dV	Change in tDQSQ versus VccQ for a LUN. Computed by dividing the delta in tDQSQ by the operating VccQ range of the device for a LUN. Spec is guaranteed by design and characterization and not tested in production.	Yes	Yes
tAC	Access window of DQ[7:0] from RE_n (RE_t/RE_c crosspoint)	Yes	Yes
tDIHL	DQ minimum input pulse width at Vcent_DQ (pin_mid) ± vDIVW_total/2	Yes	Yes
tDIPW	DQ input pulse width at Vcent_DQ (pin_mid) or VrefQ	Yes	Yes
tDIVW1	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid)	Yes	Yes
tDIVW2	DQ Rx Mask Timing Window at Vcent_DQ (pin_mid) ± vDIVW_total/2	Yes	Yes
tDQ2DQ	Maximum allowable skew between DQ signals at the NAND ball for a single LUN.	Yes	Yes
tDQDQ	Worst case DQ-to-DQ variation for a LUN during data output cycles.	Yes	Yes
tDQS2DQ	Allowable skew between DQS and DQ at the NAND ball for a single LUN.	Yes	Yes
tDQS2DQ_temp	DQ to DQS offset temperature variation	Yes	Yes
tDQS2DQ_volt	DQ to DQS offset voltage variation	Yes	Yes
tDQSD	(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device	Yes	No
tDQSH (abs)	Absolute DQS high level width	Yes	Yes
tDQSH (avg)	Average DQS high level width	Yes	Yes
tDQSL (abs)	Absolute DQS low level width	Yes	Yes
tDQSL (avg)	Average DQS low level width	Yes	Yes
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per access	Yes	Yes
tDQSRE	Access window of DQS from RE_n (RE_t/RE_c)	Yes	Yes
tDQSRH	DQS hold time after (RE_n low or RE_t/RE_c crosspoint)	Yes	No
tDSC(avg)	Average DQS cycle time	Yes	Yes
tDSC(abs)	Absolute write cycle period, measured from rising edge to the next consecutive rising edge	Yes	Yes
tDVWd	Output data valid window per device (across all IO pins)	Yes	Yes
tDVWp	Output data valid window per IO pin	Yes	Yes
tJITper	The deviation of a given tRC(abs)/tDSC(abs) from tRC(avg)/tDSC(avg)	Yes	Yes
tJITcc	Cycle-to-cycle jitter	Yes	Yes
tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access	Yes	Yes
tQSH	DQS output high time (if differential, DQS_t is high)	Yes	Yes
tQSL	DQS output low time (if differential, DQS_t is low)	Yes	Yes
tRC(avg)	Average read cycle time, also known as tRC	Yes	Yes

tRC(abs)	Absolute read cycle period, measured from rising edge to the next consecutive rising edge	Yes	Yes
tREH(abs)	Absolute RE_n/RE_t high level width	Yes	Yes
tREH(avg)	Average RE_n/RE_t high level width	Yes	Yes
tRP(abs)	Absolute RE_n/RE_t low level width	Yes	Yes
tRP(avg)	Average RE_n/RE_t low level width	Yes	Yes
tRPRE2	Read preamble	Yes	Yes
tRPST	Read postamble	Yes	No, replaced by tRPST_CA in SCA protocol
tRPSTH	Read postamble hold time	Yes	No, replaced by tRPSTH_CA in SCA protocol
tWPRE2	DQS write preamble	Yes	Yes
tWPST	DQS write postamble	Yes	No, replaced by tWPST_CA in SCA protocol
tWPSTH [1]	DQS write postamble hold time	Yes	No, replaced by tWPSTH_CA in SCA protocol
NOTE: 1. In the Conv. Protocol, for a data input burst followed by a confirm command, at the end of the burst with CLE going HIGH, WE# must toggle LOW only after meeting tWPSTH (min) timing. 2. This table does not list all data burst related timing parameters for the SCA protocol. See SCA Protocol section for other data burst related timing parameters.			

Table 4-33 Data Burst Related Timing Parameter Descriptions

4.14.3. NAND/Controller DQ Rx Mask Definition

The DQ input receiver (Rx) mask defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property and is not the valid data-eye. The DQ Rx mask for voltage and timing is shown in the figure below and is applied per individual DQ pin. Note that the DQ Rx mask also applies to the DBI signal.

The DQ Rx mask is evaluated at the die pads and Rx mask values are guaranteed with DFE disable case only. When DFE is enabled, DFE setting vs. coefficient values will be supplied by the NAND vendor. User can apply the co-efficient to/on the input signal measured at the NAND die pads. The exact pass/fail criteria after co-efficient application can be supplied by the NAND vendor.

The minimum DQ AC input pulse amplitude (pk-pk) is given by the VIHL_AC specification. The DQ only input pulse amplitude must meet or exceed VIHL_AC at least one time over the total UI, except when no transitions are occurring for that UI. VIHL_AC is centered around Vcent_DQ (pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ (pin_mid). There are no timing requirements above or below VIHL_AC levels.

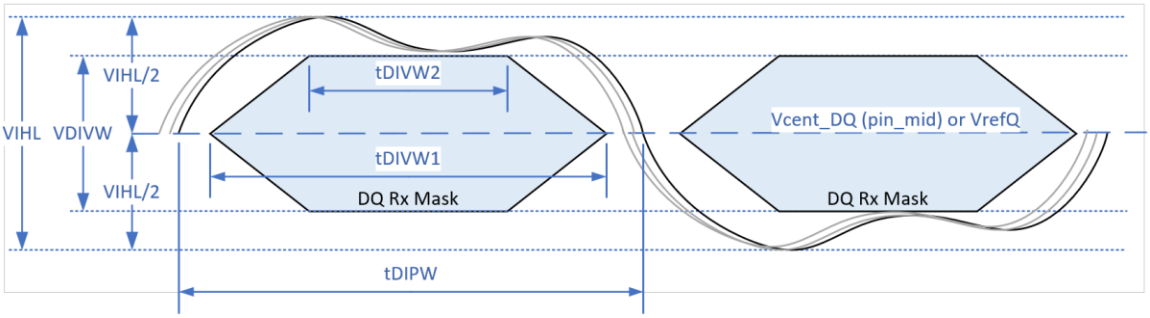


Figure 4-19 DQ Rx Mask and VIHL Definition

Vcent_DQ (pin_mid) is defined as the midpoint between the highest Vcent_DQ voltage level and the lowest Vcent_DQ voltage level across all DQ pins for a given NAND die. Each Vcent_DQ is defined by the center (ie. widest opening) of the cumulative data input eye as depicted in the figure below. Since the DQ Rx mask is centered around Vcent_DQ (pin_mid), any pin-to-pin Vcent_DQ variation must be accounted for in the DQ Rx Mask.

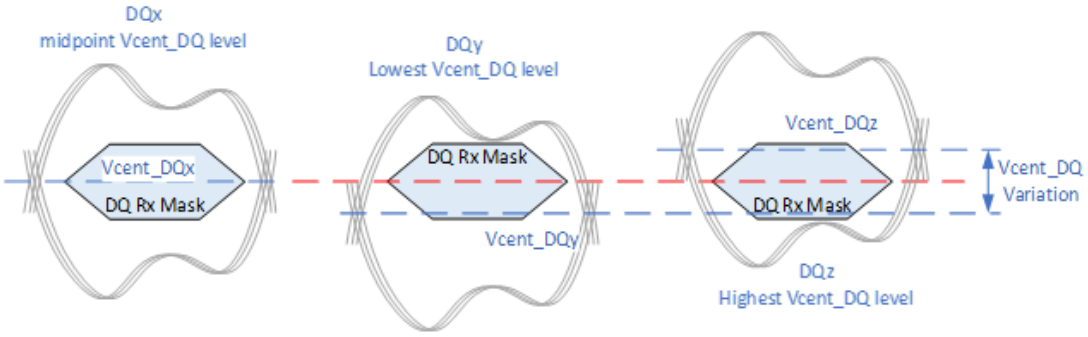


Figure 4-20 Vcent_DQ (pin_mid) Definition

4.14.4. Input Pulse Width Specifications

The tDIPW specification describes the required minimum DQ input pulse width at Vcent_DQ(pin_mid) while the tDIHL specification describes the minimum DQ input pulse width at Vcent_DQ(pin_min) ± vDIVW/2. The relationship between the two specifications is illustrated in the diagram below:

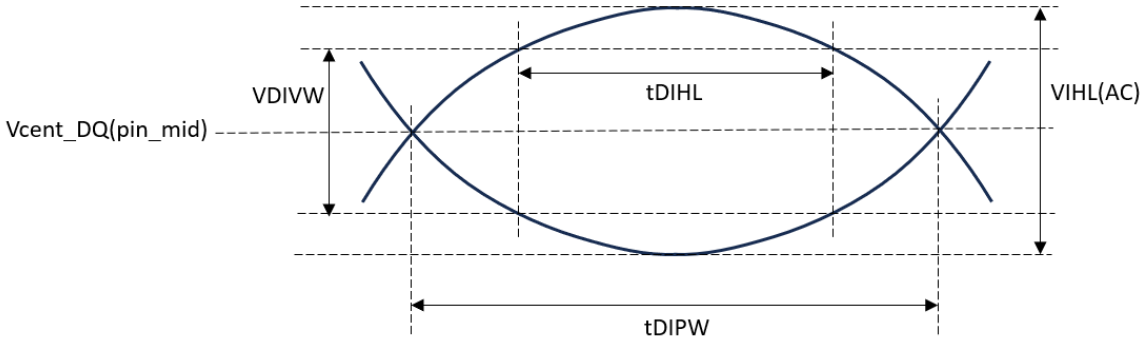


Figure 4-21 Input Pulse Width Specifications (tDIPW and tDIHL)

4.15. Timing Modes and Parameter Values

Timing modes represent speed bins for the NAND device. The host is not required to have a period that exactly matches the tDSC or tRC values listed for the standard timing modes. The host shall meet the setup and hold times and DQ Rx Mask requirements for the timing mode selected. If the host operates the NAND device in timing mode *n*, then its tDSC and tRC values shall be faster than the tDSC and tRC values of timing mode *n-1* and slower than or equal to the tDSC and tRC values of timing mode *n*.

Please refer to the Test Conditions section for the testing conditions for the various timing modes. In addition, the appropriate data trainings to support a certain timing mode must be done prior to testing the capability of the device to operate at a certain timing mode.

The following requirements apply to the timing parameter values:

1. tCHZ and tCLHZ are not referenced to a specific voltage level but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg)/tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJITper.
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and RP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter, Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter (tJITper) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC over any 200 consecutive periods. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter (tJITcc) is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle (tRP(abs) and tREH(abs) not less than 45 percent of the average cycle for ≥800 MTs with no training).
8. When the device is operated with input RE_n (RE_t/RE_c) jitter, tQSL, tQSH, and tQH need to be derated by the actual input duty cycle jitter beyond 0.45 * tRC(avg) but not exceeding 0.43 * tRC(avg) for less than 800 MT/s operation. Output deratings are relative to the device input RE_n pulse that generated the DQS pulse. For operation above 800 MT/s, even with input RE jitter, tREH(abs) and tRP(abs) should not go lower than 0.43 * tRC(avg).”
9. Minimizing the amount of duty cycle jitter to more than 45% of the average cycle provides a larger tQH, which in turn provides a larger data valid window. The device shall provide a

minimum of 0.5% of larger data valid window for each 1% improvement in duty cycle jitter. For example, if the host provides a tREH(abs) of 0.49 * tRC(avg) then the device shall provide at least a tQH of 0.39 * tRC(avg).

10. The parameter tDIPW is defined as the pulse width of the input signal between the first crossing of Vcent_DQ (pin_mid) and the consecutive crossing of Vcent_DQ (pin_mid).
11. For data rates up to 1200MT/s, parameters tDQSQ and tQH are used to calculate overall tDVWd (tDVWd = tQH - tDQSQ). tDVWd is the data valid window per device per UI and is derived from [tQH – tDQSQ] of each UI on a pin per device. Since data eye training to optimize strobe placement is expected at high I/O speeds (≥533 MT/s), tDQSQ and tQH may borrow time from each other without changing tDVWd. For example, if there exists X ps of margin on tDQSQ then tQH can be provided with an additional X ps without changing the value of tDVWd. When timing margin is borrowed from tDQSQ to provide additional timing for tQH, the same amount of timing margin can be used for additional timing for tQSL/tQSH. For data rates >1200MT/s, the tDVWp spec shall be used instead for the NAND output valid window. NAND devices may require that DCC training be done to be able to meet tDVWp (per pin valid window) requirements for >800 MT/s data rates. In order for a system to take advantage of the wider tDVWp (per pin valid window) data-eye opening versus tDVWd (overall valid window), the system must employ the ability to de-skew each individual DQ pin against DQS with Read Training.
12. For greater than 800MTs, warmup cycle(s) are required for both data input and output.
13. Both tDQS2DQ and tDQ2DQ are parameters used only when Write DQ training is supported. TDQS2DQ is the maximum allowable skew between DQS and DQ at the NAND package ball, while TDQ2DQ is the maximum allowable skew between DQ signals on a single LUN at the NAND package ball. The controller should be capable of compensating for the maximum amount of TDQS2DQ and TDQ2DQ skew during write training. The optional Write Training (RX side) mode though is not required to compensate for the maximum TDQS2DQ and TDQ2DQ amount of skew. Even with tDQS2DQ and tDQ2DQ, tDIPW still needs to be met.

Constant Timing Parameter Values			
	Min	Max	Unit
tADL	412	—	ns
tCAH	5	—	ns
tCAS	5	—	ns
tCALH	5	—	ns
tCALS	15	—	ns
tCEH	20	—	ns
tCH	5	—	ns
tCS	20	—	ns
tCS1	30	—	ns
tCS2	40	—	ns
tCSD	10	—	ns
tCHZ	—	30	ns
tCLHZ	—	30	ns
tCLR	10	—	ns
tCR	10	—	ns
tCR2	100	—	ns
tCR2 (Read ID)[1]	150	—	ns
tDBS	5	—	ns
tRHW	100	—	ns
tWC	25	—	ns
tWH	11	—	ns
tWP	11	—	ns
tWHR	80	—	ns
tWHRT	400	—	ns
tWTRN	—	200	µs
tWW	100	—	ns
tFEAT	—	1	µs
tRST	—	18/30/500	µs
tRR	20	—	ns
tWB	—	100	ns

NOTE:
1. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.
2. Some specs in this table are only applicable to the Conv. Protocol, while some are applicable to both Conv. and SCA protocols. See General Timing Parameters section for spec applicability.
3. The specs in this table apply to both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT)

Table 4-34 Command and Address Timing Parameter Values

Timing Mode Specific Values (Modes 0-3)									
	Mode 0		**Mode 1**		**Mode 2**		**Mode 3**		**Unit**
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	ns
tJITper (RE_n)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	ns
tJITcc (DQS)	—	4.8	—	4.0	—	2.4	—	2.0	ns
tJITcc (RE_n)	—	3.6	—	3.0	—	1.8	—	1.5	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.80	0.80	-0.60	0.60	-0.48	0.48	-0.40	0.40	ns
tJITper(RE_n)	-0.60	0.60	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns
tJITcc(DQS)	—	1.6	—	1.2	—	0.96	—	0.8	ns
tJITcc(RE_n)	—	1.2	—	0.9	—	0.72	—	0.6	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.30	0.30	-0.24	0.24	-0.2	0.2	-0.094	0.094	ns
tJITper(RE_n)	-0.225	0.225	-0.18	0.18	-0.15	0.15	-0.094	0.094	ns
tJITcc(DQS)	—	0.6	—	0.48	—	0.4	—	0.188	ns
tJITcc(RE_n)	—	0.45	—	0.36	—	0.3	—	0.188	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.083	0.083	-0.078	0.078	-0.075	0.075	-0.070	0.070	ns
tJITper(RE_n)	-0.083	0.083	-0.078	0.078	-0.075	0.075	-0.070	0.070	ns
tJITcc(DQS)	—	0.167	—	0.156	—	0.150	—	0.140	ns
tJITcc(RE_n)	—	0.167	—	0.156	—	0.150	—	0.140	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.062	0.062	-0.056	0.056	-0.051	0.051	-0.047	0.047	ns
tJITper(RE_n)	-0.062	0.062	-0.056	0.056	-0.051	0.051	-0.047	0.047	ns
tJITcc(DQS)	—	0.124	—	0.112	—	0.102	—	0.094	ns
tJITcc(RE_n)	—	0.124	—	0.112	—	0.102	—	0.094	ns
Timing Mode Specific Values (Mode 20-23)									
	Mode 20		**Mode 21**		**Mode 22**		**Mode 23**		**Unit**
	0.714		0.625		0.555		0.500		ns
	1400		1600		1800		2000		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tJITper(DQS)	-0.032	0.032	-0.028	0.028	-0.025	0.025	-0.023	0.023	ns
tJITper(RE_n)	-0.032	0.032	-0.028	0.028	-0.025	0.025	-0.023	0.023	ns
tJITcc(DQS)	—	0.064	—	0.056	—	0.050	—	0.046	ns
tJITcc(RE_n)	—	0.064	—	0.056	—	0.050	—	0.046	ns
Timing Mode Specific Values (Mode 24-26)									
	Mode 24		**Mode 25**		**Mode 26**				**Unit**

	0.476		0.455		0.417				ns
	2100		2200		2400				Mhz
	Min	Max	Min	Max	Min	Max			
tJITper(DQS)	-0.021	0.021	-0.020	0.020	-0.019	0.019			ns
tJITper(RE_n)	-0.021	0.021	-0.020	0.020	-0.019	0.019			ns
tJITcc(DQS)	—	0.042	—	0.040	—	0.038			ns
tJITcc(RE_n)	—	0.042	—	0.040	—	0.038			ns

NOTE:

1. The specs in this table are applicable to Conv. and SCA Protocols
2. The specs in this table are applicable to both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces

Table 4-35 Jitter Timing Parameter Values

Constant Timing Parameter Values									
	Min			Max				Unit	
tCALQS2[2]	25			—				ns	
tCDQSS[2]	30			—				ns	
tCDQSH[2]	100			—				ns	
tCD[2]	100			—				ns	
tDIHL	tDIPW – (tDIVW1 - tDIVW2)			—				ns	
tDSC(abs)	tDSC(avg) + tJITper(DQS) min			tDSC(avg) + tJITper(DQS) max				ns	
tDQ2DQ	—			0.150				ns	
tDQS2DQ	0.100			1.100				ns	
tDQS2DQ_temp	—			0.85				ps/°C	
tDQS2DQ_volt	—			0.85				ps/mV	
tWPRE2	25			—				ns	
tWPST[2]	6.5			—				ns	
tWPSTH[2]	25			—				ns	
Timing Mode Specific Values (Modes 0-3)									
	Mode 0		**Mode 1**		**Mode 2**		**Mode 3**		**Unit**
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.31	—	0.31	—	0.31	—	0.31	—	tDSC(avg)
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	30	—	25	—	15	—	12	—	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.31	—	0.31	—	0.31	—	0.31	—	tDSC(avg)
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	10	—	7.5	—	6	—	5	—	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.31	—	0.31	—	0.31	—	0.33	—	tDSC(avg)
tDQSH (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.45	—	0.45	—	0.45	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	3.75	—	3	—	2.5	—	1.875	—	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns

	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQSH (abs)	0.45	—	0.448	—	0.445	—	0.444	—	tDSC(avg)
tDQSL (abs)	0.45	—	0.448	—	0.445	—	0.444	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	1.667	—	1.5	—	1.364	—	1.25	—	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.48	—	0.48	UI
tDIVW2	—	0.30	—	0.30	—	0.30	—	0.30	UI
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQSH (abs)	0.444	—	0.444	—	0.444	—	0.444	—	tDSC(avg)
tDQSL (abs)	0.444	—	0.444	—	0.444	—	0.444	—	tDSC(avg)
tDQSH (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDQSL (avg)	—	—	—	—	—	—	—	—	tDSC(avg)
tDSC(avg) or tDSC	1.111	—	1	—	0.909	—	0.833	—	ns
Timing Mode Specific Values (Mode 20-23)									
	Mode 20		**Mode 21**		**Mode 22**		**Mode 23**		**Unit**
	0.714		0.625		0.555		0.500		ns
	1400		1600		1800		2000		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.48	—	0.48	—	0.41	—	0.41	UI
tDIVW2	—	0.30	—	0.30	—	0.23	—	0.23	UI
tDIPW	0.33	—	0.33	—	0.33	—	0.33	—	tDSC(avg)
tDQSH (abs)	0.455	0.545	0.455	0.545	0.455	0.545	0.455	0.545	tDSC(avg)
tDQSL (abs)	0.455	0.545	0.455	0.545	0.455	0.545	0.455	0.545	tDSC(avg)
tDQSH (avg)	0.475	0.525	0.475	0.525	0.475	0.525	0.475	0.525	tDSC(avg)
tDQSL (avg)	0.475	0.525	0.475	0.525	0.475	0.525	0.475	0.525	tDSC(avg)
tDSC(avg) or tDSC	0.714	—	0.625	—	0.555	—	0.500	—	ns
Timing Mode Specific Values (Mode 24-26)									
	Mode 24		**Mode 25**		**Mode 26**				**Unit**
	0.476		0.455		0.417				ns
	2100		2200		2400				MHz
	Min	Max	Min	Max	Min	Max			
tDIVW1	—	0.41	—	0.41	—	0.41			UI
tDIVW2	—	0.23	—	0.23	—	0.23			UI
tDIPW	0.33	—	0.33	—	0.33	—			tDSC(avg)
tDQSH (abs)	0.455	0.545	0.455	0.545	0.455	0.545			tDSC(avg)
tDQSL (abs)	0.455	0.545	0.455	0.545	0.455	0.545			tDSC(avg)
tDQSH (avg)	0.475	0.525	0.475	0.525	0.475	0.525			tDSC(avg)
tDQSL (avg)	0.475	0.525	0.475	0.525	0.475	0.525			tDSC(avg)
tDSC(avg) or tDSC	0.476	—	0.455	—	0.417	—			ns

NOTE:
1. Unit Interval (UI) is 0.5*tDSC(avg).
2. Specs apply to Conv. Protocol only
3. Unless otherwise noted, specs in this table apply to both Conv. and SCA Protocols
4. Unless otherwise noted, specs in this table apply to both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces

Table 4-36 Data Input Timing Parameter Values

The Controller DQ RX Mask specifications in the following table are applicable to controllers that support the data rates listed. These specifications do not apply to the NAND component.

Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.40	—	0.40	—	0.40	—	0.40	UI
tDIVW2	—	0.25	—	0.25	—	0.25	—	0.25	UI
tDIPW	0.25	—	0.25	—	0.25	—	0.25	—	tDSC(avg)
Timing Mode Specific Values (Mode 20-23)									
	Mode 20		**Mode 21**		**Mode 22**		**Mode 23**		**Unit**
	0.714		0.625		0.555		0.500		ns
	1400		1600		1800		2000		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDIVW1	—	0.40	—	0.40	—	0.40	—	0.35	UI
tDIVW2	—	0.25	—	0.25	—	0.25	—	0.18	UI
tDIPW	0.25	—	0.25	—	0.25	—	0.225	—	tDSC(avg)
Timing Mode Specific Values (Mode 24-26)									
	Mode 24		**Mode 25**		**Mode 26**				**Unit**
	0.476		0.455		0.417				ns
	2100		2200		2400				Mhz
	Min	Max	Min	Max	Min	Max			
tDIVW1	—	0.35	—	0.35	—	0.35			UI
tDIVW2	—	0.18	—	0.18	—	0.18			UI
tDIPW	0.225	—	0.225	—	0.225	—			tDSC(avg)

NOTE:
1. Unit Interval (UI) is 0.5*tDSC(avg).
2. At 1600Mbps and below, use of Rx mask specifications is optional, see vendor datasheet whether Rx mask specifications are supported by the device at that data rate.
3. The controller DQ Rx mask specification is only for reference and smaller value might be required depending on system. System designers should use IBIS model to close overall system timings.
4. Unless otherwise noted, specs in this table apply to both Conv. and SCA Protocols
5. Unless otherwise noted, specs in this table apply to both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces

Table 4-37 Controller NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT) Interface RX Mask Timing Specifications

Constant Timing Parameter Values			
	Min	Max	Unit
dQSQ/dT	-0.5	0.5	ps/°C
dQSQ/dV	-0.35	0.35	ps/mv
tCALR2[1]	25	—	ns
tDQSD	5	18	ns
tDVWd (device)	tDVWd = tQH – tDQSQ (TM0-TM12)		ns
tQH	0.37 (TM0-TM12)	—	tRC(avg)
tQSH	0.37	—	tRC(avg)
tQSL	0.37	—	tRC(avg)
tRC(abs)	tRC(avg) + tJITper(RE_n) min	tRC(avg) + tJITper(RE_n) max	ns
tRPRE2 (Conv. Protocol)	25	—	ns
tRPRE2 (SCA Protocol)	See SCA section for spec value	—	ns
tRPST[1]	tDQSRE + 0.5*tRC	—	ns
tRPSTH[1]	15	—	ns
tDQSRH[1]	3	5	ns

Timing Mode Specific Values (Modes 0-3)									
	Mode 0		Mode 1		Mode 2		Mode 3		Unit
	30		25		15		12		ns
	~ 33		40		~ 66		~ 83		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	2.5	—	2.0	—	1.4	—	1.0	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	30	—	25	—	15	—	12	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	NA	—	ns
tAC	1.0	25	1.0	25	1.0	25	1.0	25	ns
tDQSRE	1.0	25	1.0	25	1.0	25	1.0	25	ns
Timing Mode Specific Values (Modes 4-7)									
	Mode 4		**Mode 5**		**Mode 6**		**Mode 7**		**Unit**
	10		7.5		6		5		ns
	100		~133		~166		200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.8	—	0.6	—	0.5	—	0.4	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	10	—	7.5	—	6	—	5	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	NA	—	ns
tAC	1.0	25	1.0	25	1.0	25	1.0	25	ns
tDQSRE	1.0	25	1.0	25	1.0	25	1.0	25	ns
Timing Mode Specific Values (Modes 8-11)									
	Mode 8		**Mode 9**		**Mode 10**		**Mode 11**		**Unit**
	3.75		3		2.5		1.875		ns
	~267		~333		400		~533		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.350	—	0.3	—	0.25	—	0.188	ns
tDQDQ	—	—	—	—	—	—	—	—	ns
tRC(avg) or tRC	3.75	—	3	—	2.5	—	1.875	—	ns
tREH/tRP(abs) (no training)	0.43	—	0.43	—	0.43	—	0.45	—	tRC(avg)
tREH/tRP(avg) (no training)	0.45	0.55	0.45	0.55	0.45	0.55	0.47	0.53	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	NA	—	NA	—	NA	—	0.535	—	ns
tAC	1.0	25	1.0	25	1.0	25	1.0	25	ns
tDQSRE	1.0	25	1.0	25	1.0	25	1.0	25	ns
Timing Mode Specific Values (Mode 12-15)									
	Mode 12		**Mode 13**		**Mode 14**		**Mode 15**		**Unit**
	1.667		1.5		1.364		1.25		ns
	600		~667		~733		800		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	—	0.167	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns

tDQDQ	—	—	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	1.667	—	1.5	—	1.364	—	1.25	—	ns
tREH/tRP(abs) (no training)	0.45	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	0.47	0.53	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	0.475	—	0.428	—	0.389	—	0.356	—	ns
tAC	1.0	25	1.0	25	1.0	25	1.0	25	ns
tDQSRE	1.0	25	1.0	25	1.0	25	1.0	25	ns
Timing Mode Specific Values (Mode 16-19)									
	Mode 16		**Mode 17**		**Mode 18**		**Mode 19**		**Unit**
	1.111		1		0.909		0.833		ns
	900		1000		1100		1200		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns
tDQDQ	—	0.200	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	1.111	—	1	—	0.909	—	0.833	—	ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tRP(abs) (with training)	0.43	—	0.43	—	0.43	—	0.43	—	tRC(avg)
tREH(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tRP(avg) (with training)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
tDVWp (per pin)	0.317	—	0.285	—	0.259	—	0.237	—	ns
tAC	1.0	25	1.0	25	1.0	25	1.0	25	ns
tDQSRE	1.0	25	1.0	25	1.0	25	1.0	25	ns
Timing Mode Specific Values (Mode 20-23)									
	Mode 20		**Mode 21**		**Mode 22**		**Mode 23**		**Unit**
	0.714		0.625		0.555		0.500		ns
	1400		1600		1800		2000		MHz
	Min	Max	Min	Max	Min	Max	Min	Max	
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250	-0.250	0.250	ns
tDQDQ	—	0.200	—	0.200	—	0.200	—	0.200	ns
tRC(avg) or tRC	0.714	—	0.625	—	0.555	—	0.500	—	ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—	—	—	tRC(avg)
tREH(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545	0.455	0.545	tRC(avg)
tRP(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545	0.455	0.545	tRC(avg)
tREH(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525	0.475	0.525	tRC(avg)
tRP(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525	0.475	0.525	tRC(avg)
tDVWp (per pin)	0.203	—	0.178	—	0.158	—	0.142	—	ns
tAC	1.0	25	1.0	25	1.0	25	1.0	25	ns
tDQSRE	1.0	25	1.0	25	1.0	25	1.0	25	ns
Timing Mode Specific Values (Mode 24-26)									
	Mode 24		**Mode 25**		**Mode 26**				**Unit**
	0.476		0.455		0.417				ns
	2100		2200		2400				MHz
	Min	Max	Min	Max	Min	Max			
tDQSQ	-0.250	0.250	-0.250	0.250	-0.250	0.250			ns
tDQDQ	—	0.200	—	0.200	—	0.200			ns
tRC(avg) or tRC	0.476	—	0.455	—	0.417	—			ns
tREH/tRP(abs) (no training)	—	—	—	—	—	—			tRC(avg)
tREH/tRP(avg) (no training)	—	—	—	—	—	—			tRC(avg)
tREH(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545			tRC(avg)
tRP(abs) (with training)	0.455	0.545	0.455	0.545	0.455	0.545			tRC(avg)
tREH(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525			tRC(avg)

tRP(avg) (with training)	0.475	0.525	0.475	0.525	0.475	0.525			ns
tDVWp (per pin)	0.135	—	0.129	—	0.118	—			ns
tAC	1.0	25	1.0	25	1.0	25			ns
tDQSRE	1.0	25	1.0	25	1.0	25			ns

NOTE:
1. Specs apply to Conv. Protocol only
2. Unless otherwise noted, specs in this table apply to both Conv. and SCA Protocols
3. Unless otherwise noted, specs in this table apply to both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces

Table 4-38 Data Output Timing Parameter Values

4.16. Timing Diagrams

This section shows the timing diagrams for each phase of an operation (command, address, data input, and data output cycles) applicable for both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces.

While the diagrams in this section are pre-dominantly for the Conv. Protocol, some diagrams in this section are also applicable to the SCA Protocol and are labelled accordingly. SCA timing diagrams are pre-dominantly found in the SCA section of this document.

4.16.1.1. Conv. Protocol Command Cycle Timings

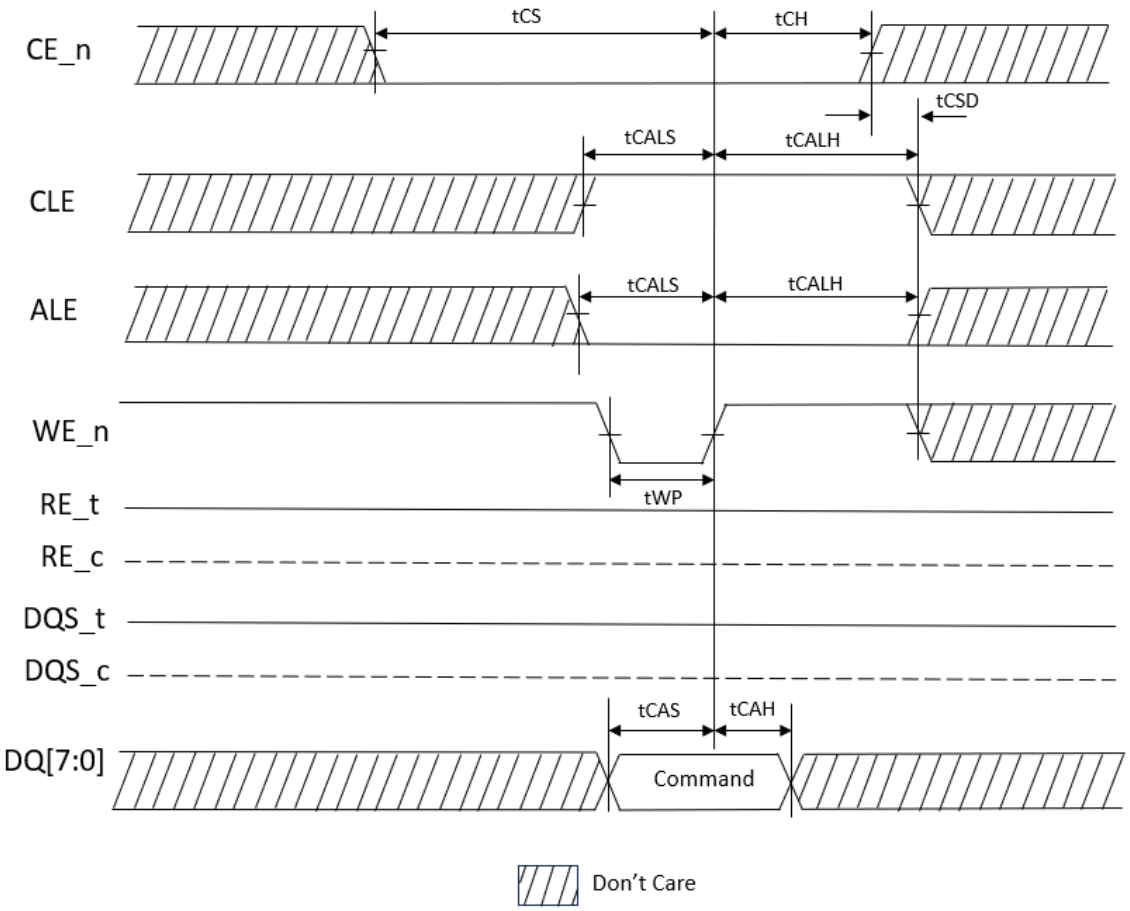


Figure 4-22 Conv. Protocol Command Cycle Timings

4.16.1.2. Conv. Protocol Address Cycle Timings

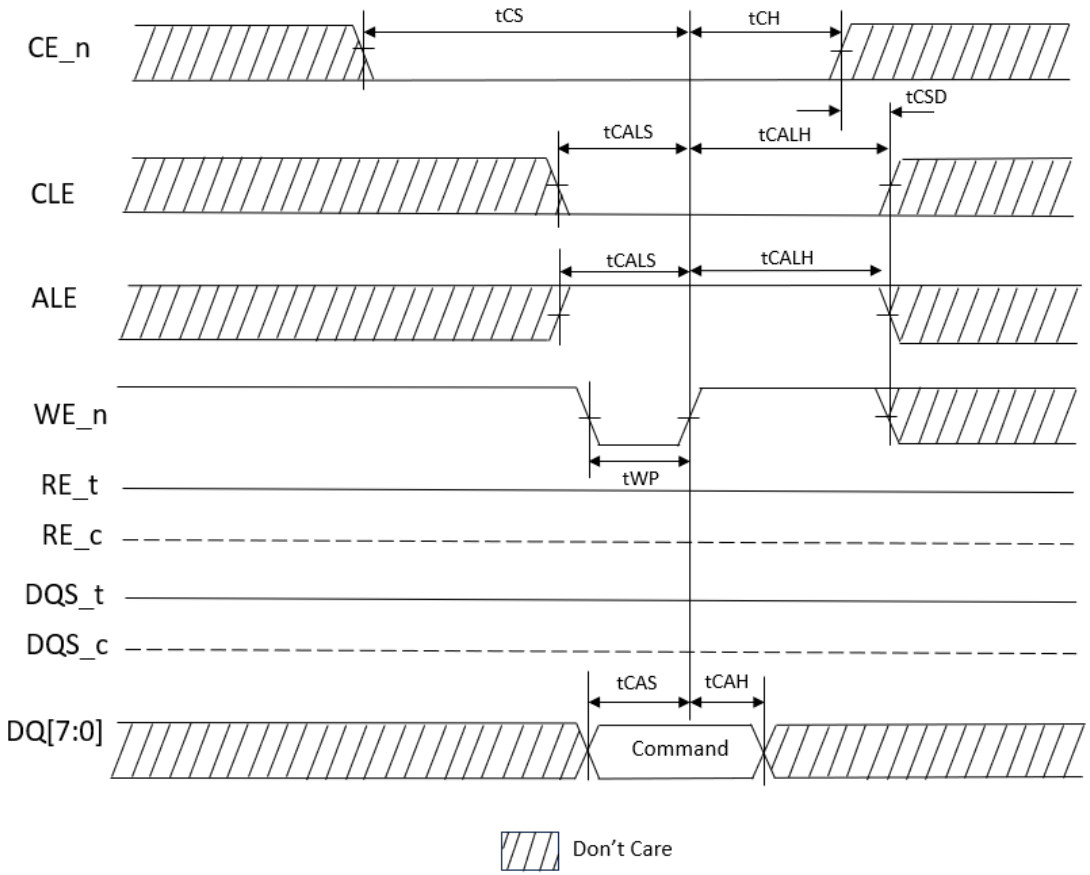


Figure 4-23 Conv. Protocol Address Cycle Timings

4.16.1.3. Conv. Protocol Data Input Cycle Timings

Data input cycle timing describes timing for data transfers from the host to the device (i.e. data writes).

For the Set Features and ODT Configure command, the same data byte is repeated twice. The data pattern in this case is D_0 D_0 D_1 D_1 D_2 D_2 etc. The device shall only latch one copy of each data byte.

ODT is not required to be used for data input. If ODT is selected for use via Set Features, then ODT is enabled and disabled during the points indicated in the following figures.

NOTE:
1. tDBS references the last falling edge of either CLE, ALE or CE_n.
2. To exit the data burst, either CE_n, ALE, or CLE is set to one by the host.

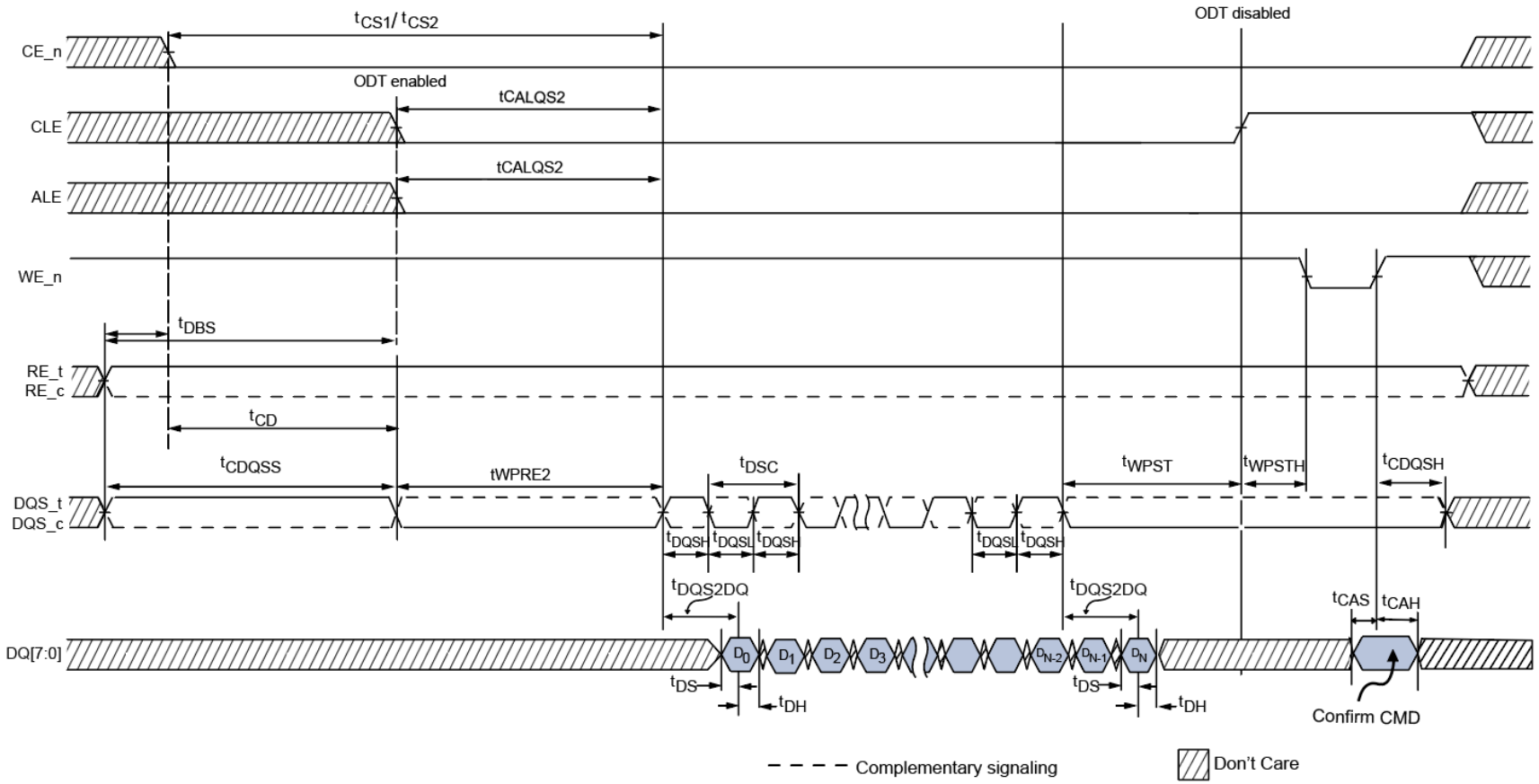


Figure 4-24 Conv. Protocol Data Input Cycle Timing

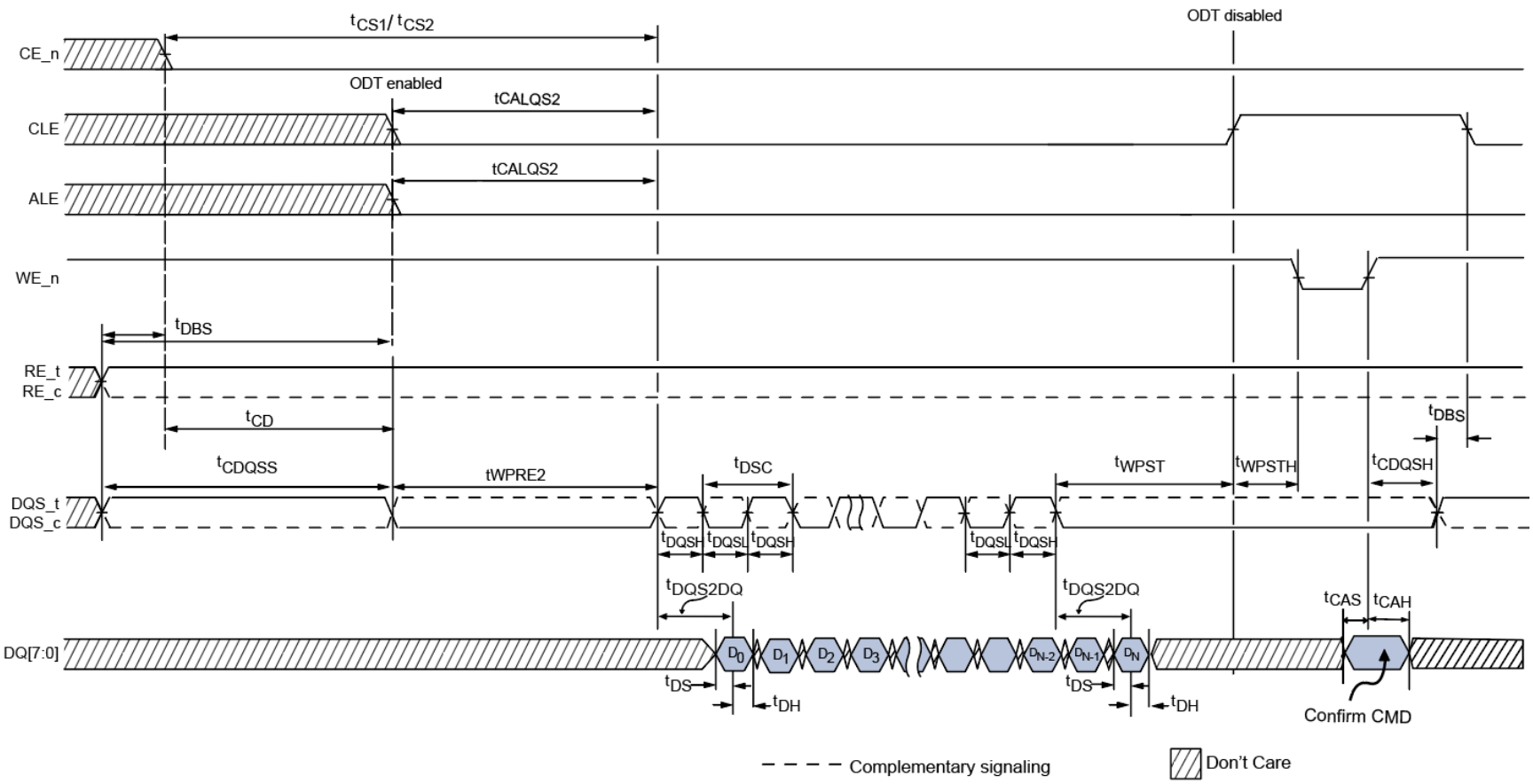


Figure 4-25 Example of Conv. Protocol Data Input Cycle Timing with CLE HIGH Burst-End with Confirm Command, tDBS Before CLE De-Assertion

4.16.1.4. Conv. Protocol Data Output Cycle Timings

Data output cycle timing describes timing for data transfers from the device to the host (i.e. data reads).

For the Read ID, Get Features, Read Status, and Read Status Enhanced commands, the same data byte is repeated twice. The data pattern in this case is D_0 D_0 D_1 D_1 D_2 D_2 etc. The host shall only latch one copy of each data byte.

ODT is not required to be used for data output. If ODT is selected for use via Set Features, then ODT is enabled and disabled during the points indicated in in the following figures.

NOTE:
1. tDBS references the last falling edge of either CLE, ALE or CE_n.
2. To exit the data burst, either CE_n, ALE, or CLE is set to one by the host. tCHZ only applies when CE_n is used to end the data burst.

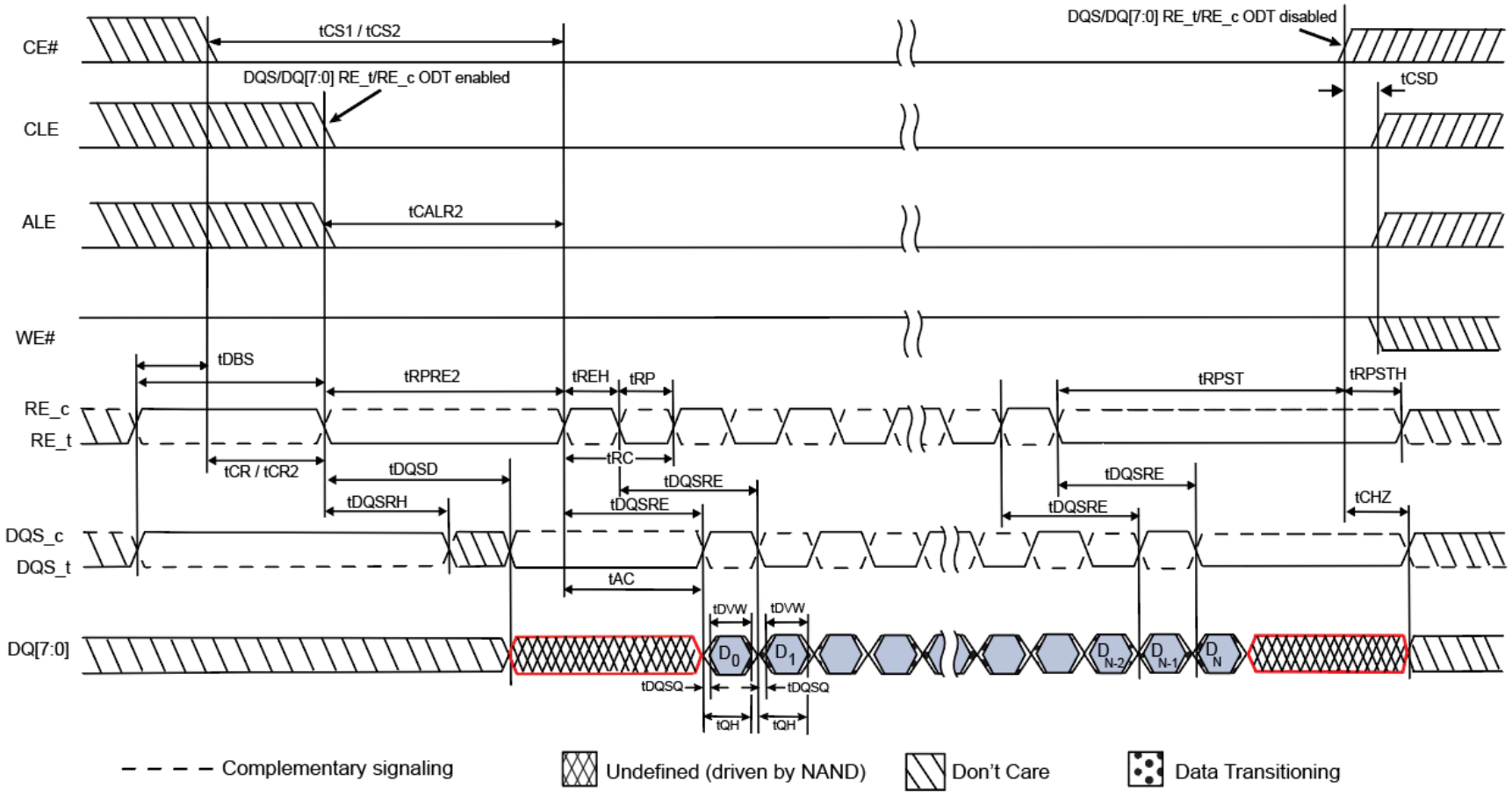


Figure 4-26 Conv. Protocol Data Output Cycle Timing

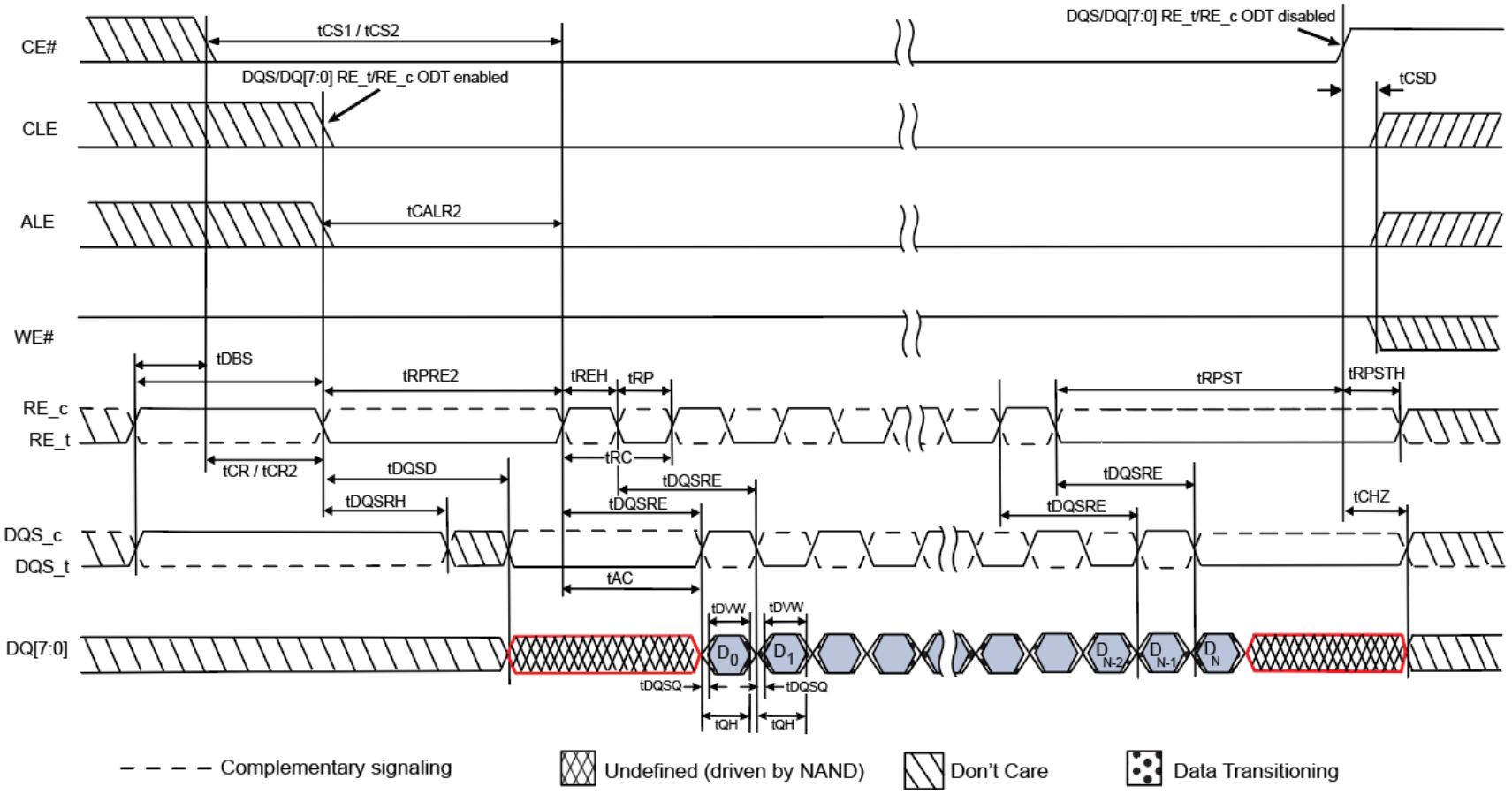


Figure 4-27 Example of Conv. Protocol Data Output Cycle Timing with CE# De-Assertion at Burst-End

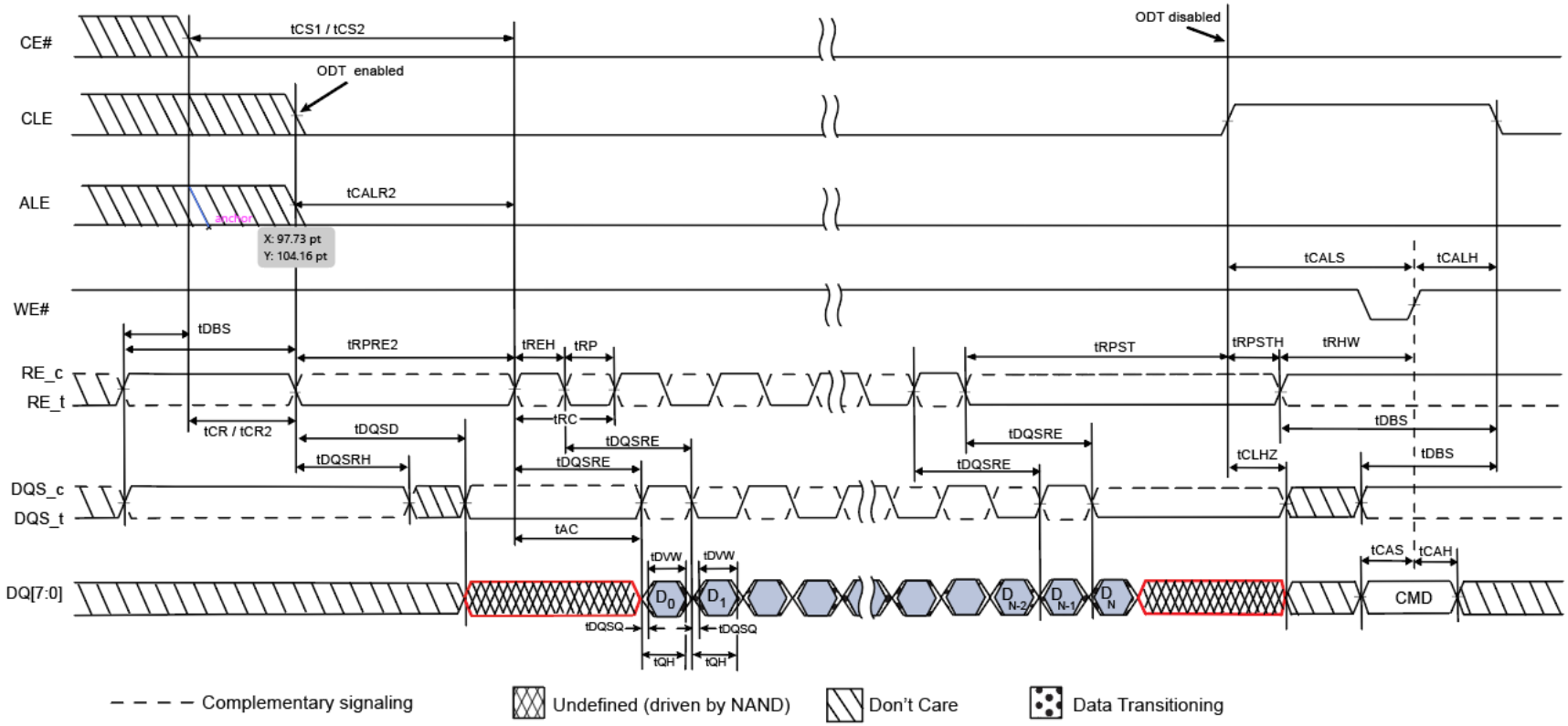


Figure 4-28 Example of Conv. Protocol Data Output Cycle Timing with CLE HIGH Burst-End Followed by Command Cycle

4.16.1.5. Conv. and SCA Protocol Data Input Skew Specs

Write DQ Training of NAND shall be used to find optimum input timing at “NAND internal latch”, not at “NAND pin”. The controller shall find the optimum input timing by timing scan between each DQ to DQS_c/DQS_t and shall compensate input timing of each DQ and DQS to be the optimum per pin per chip.

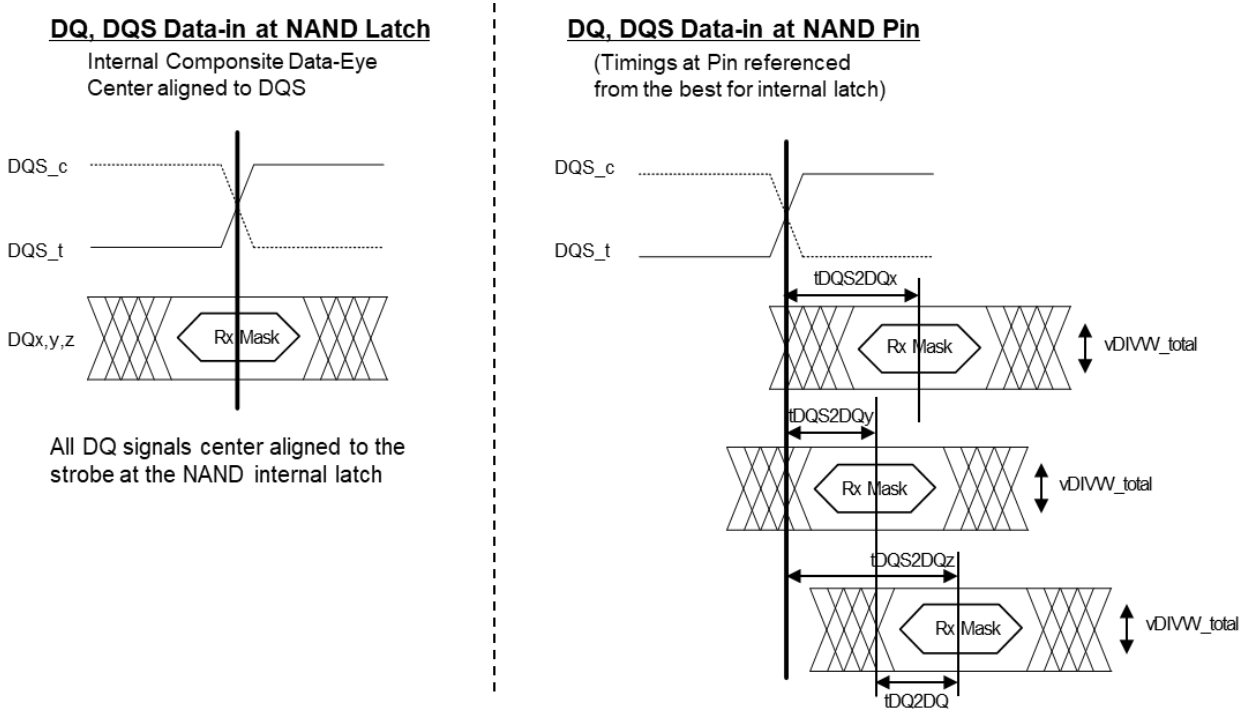


Figure 4-29 Conv. and SCA Protocol Data Input Skew Timings

The device uses an unmatched DQS-DQ path to enable high-speed performance. The DQS strobe must be trained to arrive at the DQ latch center-aligned with the data eye. The DQ receiver is located at the DQ pad and has a shorter internal delay than the DQS signal. The DQ receiver will latch the data present on the DQ bus when DQS reaches the latch and write DQ training is accomplished by delaying the DQ signals relative to DQS such that the data eye arrives at the NAND internal latch centered on the DQS transition.

The DQ-to-DQS tDQS2DQ and tDQ2DQ timings are measured from the DQS_t/DQS_c cross-point to the center of the DQ Rx Mask. The timings at the pins are referenced with respect to all DQ signal center-aligned at the NAND internal latch. The data-to-data offset is defined as the difference between the min and max tDQS2DQ for a given component.

As temperature and voltage change on the NAND die, the DQS clock tree will shift and may require retraining. The DQS oscillator feature is used to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time.

4.16.1.6. Conv. and SCA Protocol Data Output Valid Window and Skew Timings

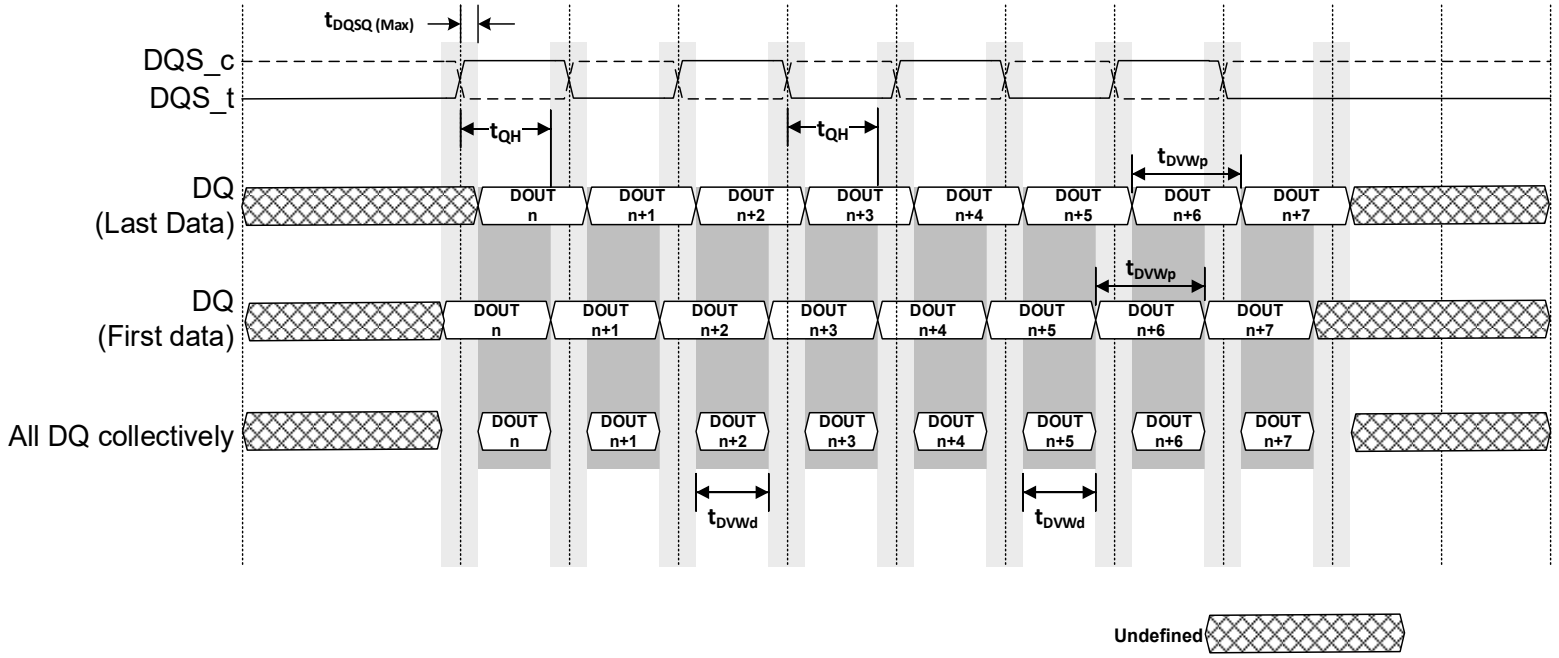


Figure 4-30 Conv. and SCA Protocol Data Output Valid Window Timing Specs: tDQSQ, tQH, tDVWd, tDVWp

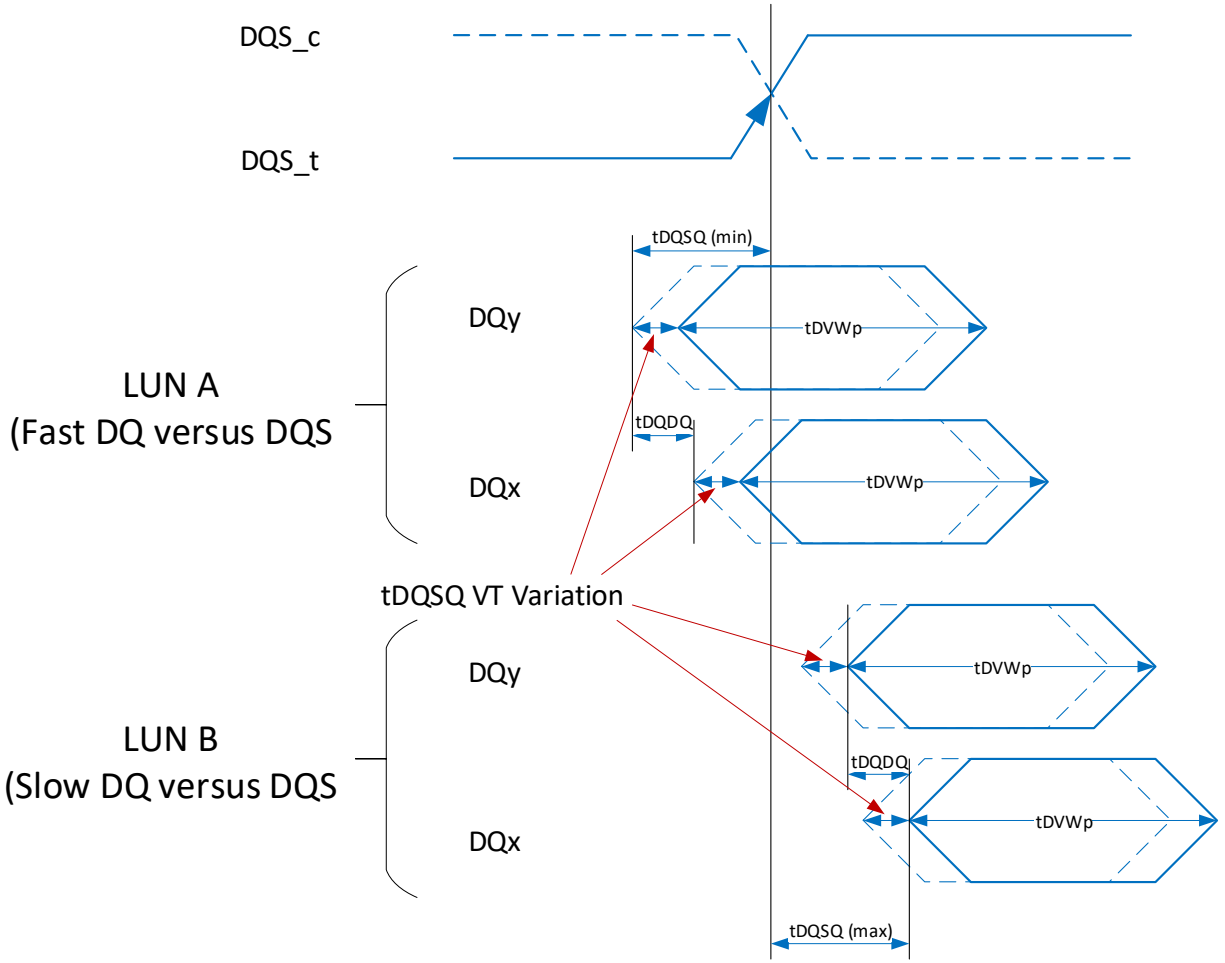


Figure 4-31 Conv. and SCA Protocol Data Output Valid Window Timing Specs for >1200MT/s: tDQSQ, tDQDQ, tDVWp

5. Separate Command Address (SCA) Protocol

5.1. Introduction

With increasing data transfer rates on the NAND interface, the command/address transfer time has not improved accordingly. To address this problem, the Separate Command Address (SCA) protocol has been defined. Compared to the legacy conventional (Conv.) protocol, the SCA protocol separates command/address (CA) and data busses, allowing concurrent command/address (CA) and data traffic, improving NAND interface efficiency.

5.2. SCA vs Conventional Protocol Comparison

Description	Conv. Protocol	SCA Protocol
NAND Pins	• ALE, CE#, CLE, WE# • Pins above are input-only	• CA[0], CA_CE#, CA[1], CA_CLK • SCA • CA_CE#, CA_CLK and SCA pins are input-only while CA[1:0] are bi-directional
Pin signaling	HSUL	HSUL
CA bus input protocol	SDR	DDR
CA bus input pins used	DQ[7:0] (CA bus same as DQ bus)	CA[1:0]
CA bus input cycle time	10ns (t_{WC} min)	4ns (t_{CACI} min)[1]
CA bus input header cycles	None	1
CA bus output protocol	SDR	Sync DDR
CA bus output pins used	DQ[7:0] (CA bus same as DQ bus)	CA[1:0]
CA bus output cycle time	Variable (prior to data training DQ bus traffic must be at slow data rate, after data training, traffic may occur at faster data rate)	10ns (t_{CACO} min)
DQ bus pins for data	DQ[7:0]	DQ[7:0]
DQ bus control	CE#	Command packets (SCE/SCP/SCT/NTO)
Protocol enable/disable	Conv. protocol enabled by default on legacy NAND devices that only support Conv. protocol	Value of SCA pad on NAND die / SCA balls on the raw NAND package on power-up determine whether Conv. or SCA protocol enabled
Program Command Sequence	80h-Addr-DIN-10h-tPROG	80h-Addr-12h-SCE-DIN-SCT-LUNSel(opt)-10h-tPROG
Non-target ODT Scheme	ODT# (nWP) pin, Matrix ODT	Non-Target ODT (NTO) Packet
Notes 1. Signal integrity analysis required to determine if minimum t_{CACI} may be used on the system		

Table 5-1 SCA vs Conventional Protocol Summary Table

5.3. SCA vs Conventional Protocol Signals

When the SCA protocol is enabled, several signals on the NAND interface change functionality and/or signal name.

The figure below shows the signal differences between the Conv. and SCA protocols at the NAND die (LUN) level:

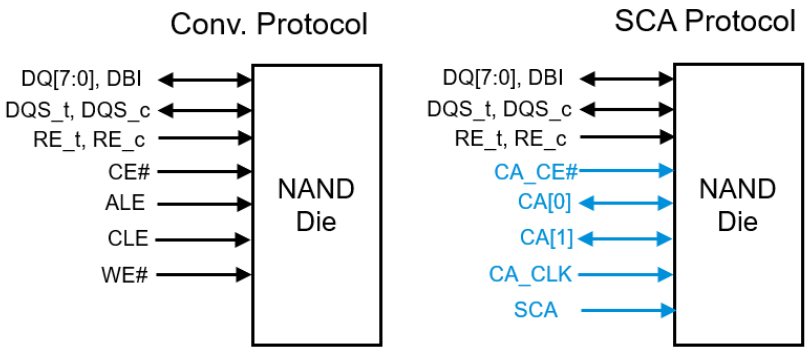


Figure 5-1 SCA vs Conventional Protocol Signals - NAND Die Level

The CE# signal in the Conv. protocol is renamed as CA_CE# in the SCA protocol to better reflect its SCA function. The WE# signal in the Conv. protocol is renamed as CA_CLK in the SCA protocol to better reflect its SCA function. The input-only ALE signal in the Conv. protocol becomes the bi-directional CA[0] signal in the SCA protocol, while the input-only CLE signal in the Conv. protocol becomes the bi-directional CA[1] signal in the SCA protocol.

The figure below shows the signal differences between the Conv. protocol versus the SCA protocol at the NAND package level using a 2-CH ODP NAND package with 4 CE# (2 CE# per package channel) as an example. As can be seen in this example, at the NAND package level, with the SCA protocol enabled, there can be multiple CA_CE# signals for each package channel.

Note: NAND packages may vary in number of channels per package and number of CE#s per package. Also, SCA_0 and SCA_1 signals may be unconnected to each other at the package level as shown in the example below, or connected to each other at the package level (not shown in the example below).

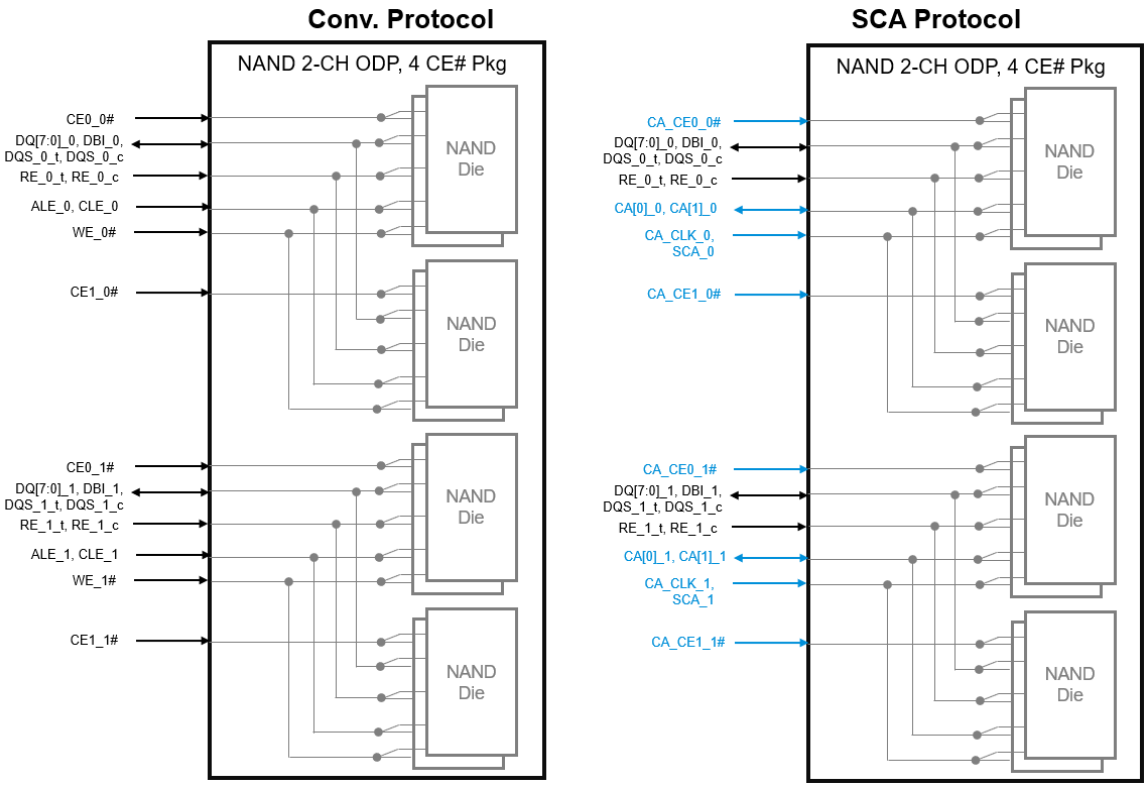


Figure 5-2 SCA vs Conventional Protocol Signals - NAND Package Level

5.4. SCA Protocl CA Bus and DQ Bus Definition and Control

When the SCA protocol is enabled, the term “CA Bus” shall collectively refer to the CA[1:0] and CA_CLK signals and the term “DQ Bus” shall collectively refer to the DQ[7:0], DBI, DQS_t, DQS_c, RE_t and RE_c signals.

In contrast to the Conv. protocol where the DQ, DQS, RE and DBI signals and control signals (ALE, CLE, WE#) are all enabled/disabled using the CE# signal, in the SCA protocol the CA_CE# signal only enables/disables the CA bus for the LUNs connected to that CA_CE#, while the DQ bus for those LUNs are enabled/disabled via packets on the CA bus. The difference in DQ bus control between Conv. and SCA protocols is illustrated in the figure below:

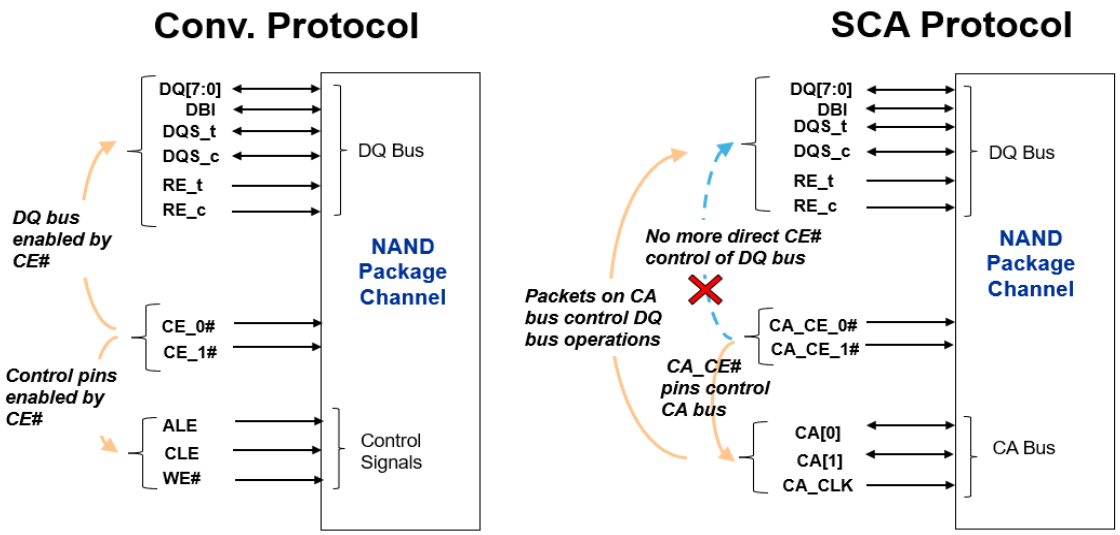


Figure 5-3 Conventional vs SCA Protocol Control of Control Pins/CA Bus and DQ Bus

5.5. SCA Protocol Enable/Disable

The SCA or Conv. protocol is enabled based on the connection of the SCA pad/SCA balls at power-up. The following table shows the protocol that is enabled versus the SCA pad/ball connection:

Protocol Enabled	SCA Pad/SCA Ball Connection
Conv. Protocol (optional)	Vss or Float
SCA Protocol	VccQ

Table 5-2 CA Protocol Versus SCA Pad/Ball Connection

See Physical Interface section for the location of SCA balls on the different NAND packages (note that there may be older NAND packages in the section which will not support SCA). When there are multiple SCA balls on a package, all SCA balls must have the same connection (ie. all Vss, or all Float, or all VccQ).

5.6. SCA Protocol Power-up Considerations

When the SCA protocol is enabled, the WE# signal becomes the CA_CLK signal. The WE# signal in the Conv. protocol is default HIGH while the CA_CLK signal in the SCA protocol is default LOW. Thus, when powering-up with the SCA protocol enabled, special consideration is needed to initialize the CA_CLK signal LOW prior to asserting CA_CE# LOW.

CA_CLK may be powered-up LOW (see Figure 5-4 SCA Protocol Power-up CA_CLK and CA_CE# Considerations, Case1), however, if CA_CLK is powered-up HIGH (see Figure 5-4 SCA Protocol Power-up CA_CLK and CA_CE# Considerations, Case 2), CA_CLK must be driven LOW t_{WLCEL_CA} prior to the first CA_CE# LOW toggle after power-up.

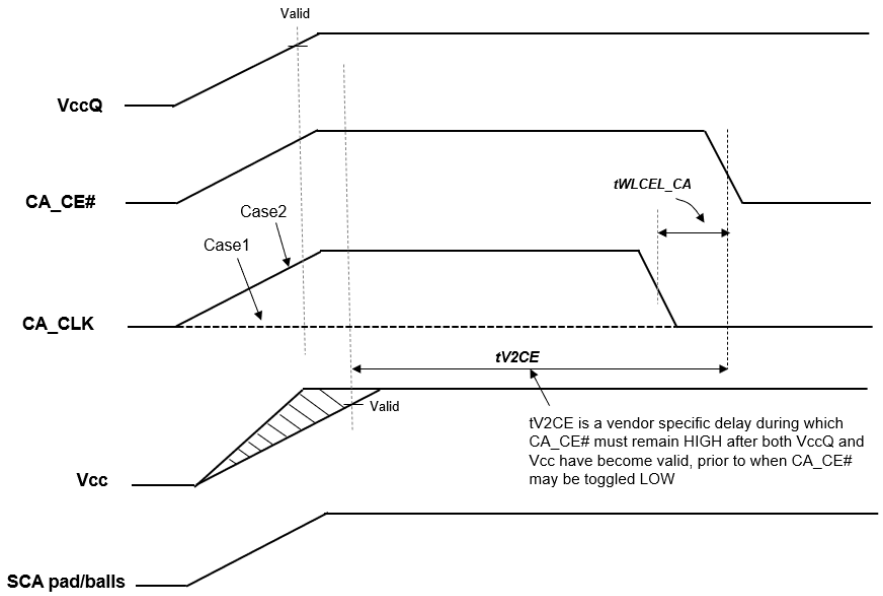


Figure 5-4 SCA Protocol Power-up CA_CLK and CA_CE# Considerations

5.7. SCA Packets and Packet Structure

Communication between the host and the NAND on the CA bus is done via packets. There are 3 CA packet structures defined in the SCA protocol:

a) CA input packet structure
b) CA output packet structure with single-byte output format
c) CA output packet structure with multi-byte output format (optional for NAND vendors to support)

5.7.1. CA Input Packet Structure

CA input packets are used to communicate command, address, and other information from the host to the NAND.

The structure of CA input packets is shown in the figure below:

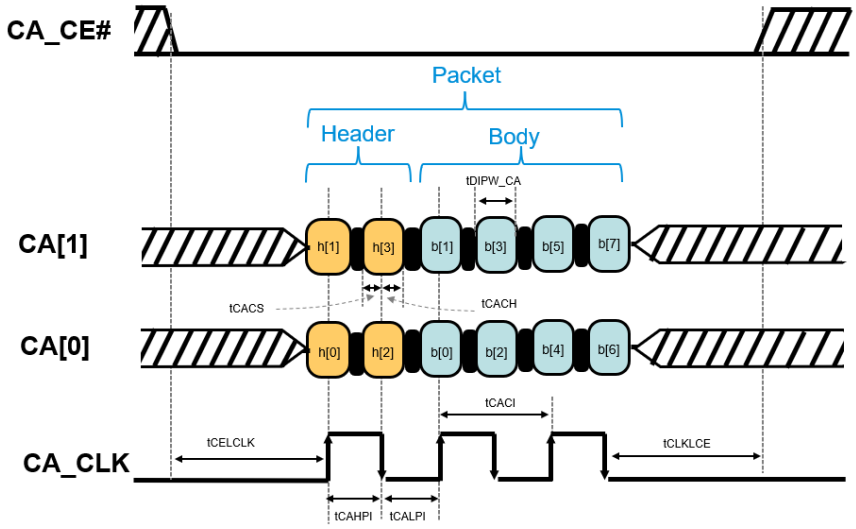


Figure 5-5 SCA CA Input Packet Structure

Each CA input packet begin with 4 bits of header information. The header allows the NAND to distinguish between different CA input packet types. See the SCA Header Definition section for the different packet types.

After the 4-bit header, 8 bits of packet body follows. The information in the packet body depends on the CA input packet type. A command packet for example contains command opcodes in the body while an address packet contains address information.

5.7.2. CA Output Packet Structure with Single Byte Output Format (Default)

CA output packets are used to communicate information from the NAND to the host. There are 2 CA output packet formats in the SCA protocol: single-byte output format and multi-byte output format. NAND vendor support for single-byte output format is mandatory, while NAND vendor support for multi-byte output format is optional.

The CA output packet format in NAND devices is controlled by the optional SCA_OUT bit in FA 02h P4[0].

SCA_OUT (optional, SCA)
This field controls the SCA protocol CA output packet format
0h (default) = single-byte CA output format
1h = multi-byte CA output format

The single-byte output format is the power-on default format for NAND devices.
The single-byte output format is shown in the figure below:

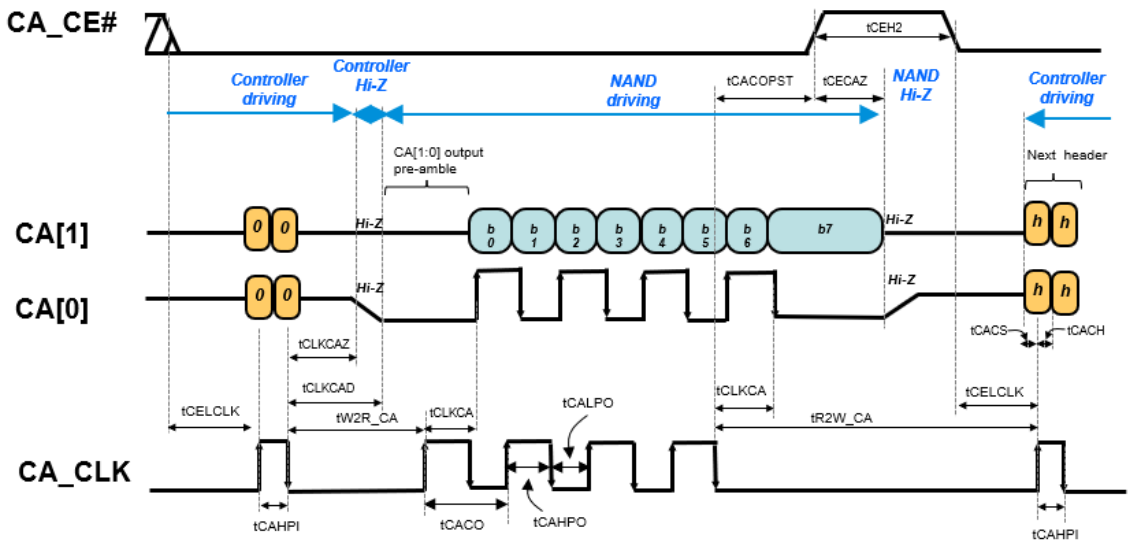


Figure 5-6 SCA CA Output Packet with Single-Byte Output Format Structure

The CA output packet begins with the host inputting the CA output header to the NAND, this puts the NAND in CA output mode. After inputting the header, the host shall then Hi-Z the CA[1:0] signals by t_{CLKCAZ}. The NAND then starts driving CA[1:0] with "00b" pre-amble data after t_{CLKCAD}. After tW2R_CA, the host toggles CA_CLK which produces a bit of output on CA[1] and the corresponding toggle on the CA[0] signal (which acts as a strobe signal during CA output mode). The host toggles CA_CLK until a byte of information has been outputted. To make the NAND exit CA output mode, the host toggles CA_CE# high, after which the NAND shall Hi-Z the CA[1:0] signals by t_{CECAZ}. The controller may then drive CA[1:0] again after t_{CECAZ} has elapsed to issue the next header.

For command sequences that produce multiple bytes of output on the CA bus (ie.Get Feature, Get Feature by LUN, Read ID), when the single-byte output format is enabled, a CA output header from the controller is required for every byte of output from the NAND. This is shown in the following Get Feature (EEh) sequence example, where multiple CA output headers are needed to output the 4 bytes of register information:

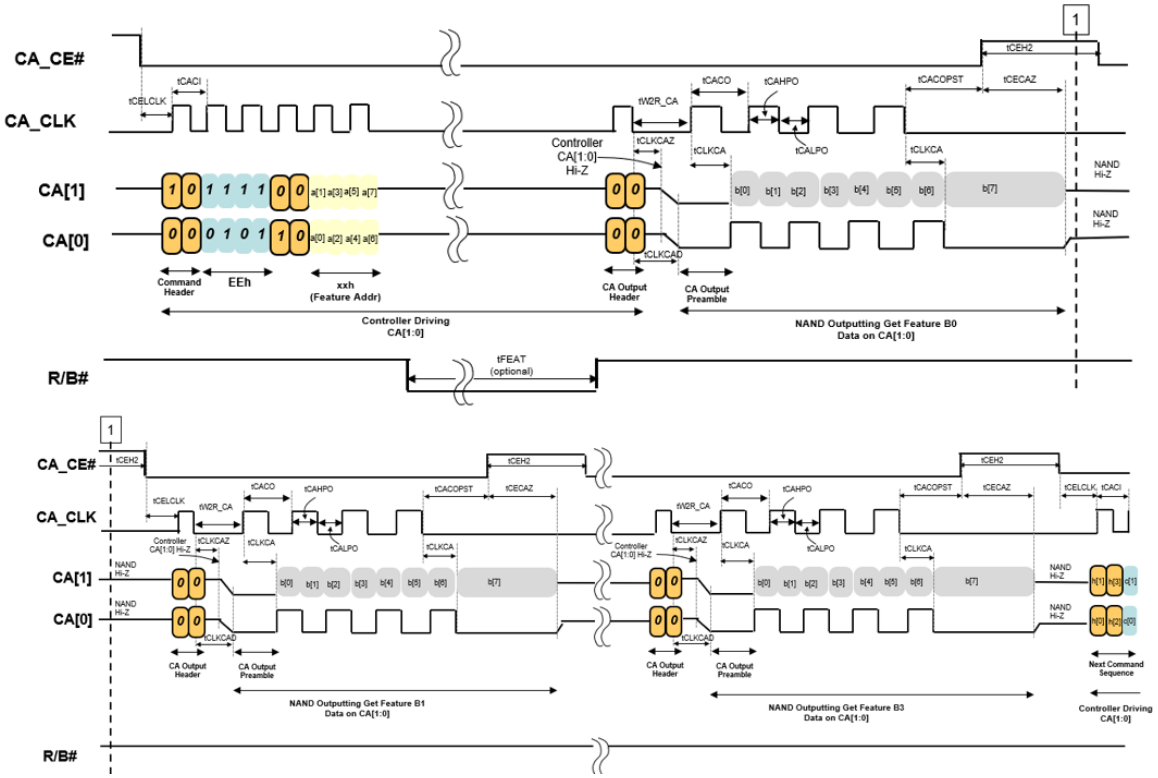


Figure 5-7 Get Feature (EEh) with Single-Byte CA Output Packet Format

5.7.3. CA Output Packet Structure with Multi-Byte Output Format (optional for NAND vendors to support)

When the multi-byte CA output packet format is enabled (SCA_OUT = 1), during command sequences that produce multiple bytes of output from the NAND on the CA bus, the NAND outputs multiple bytes of data on the CA bus with just a single header issuance from the controller. This is shown in the Get Feature (EEh) sequence below:

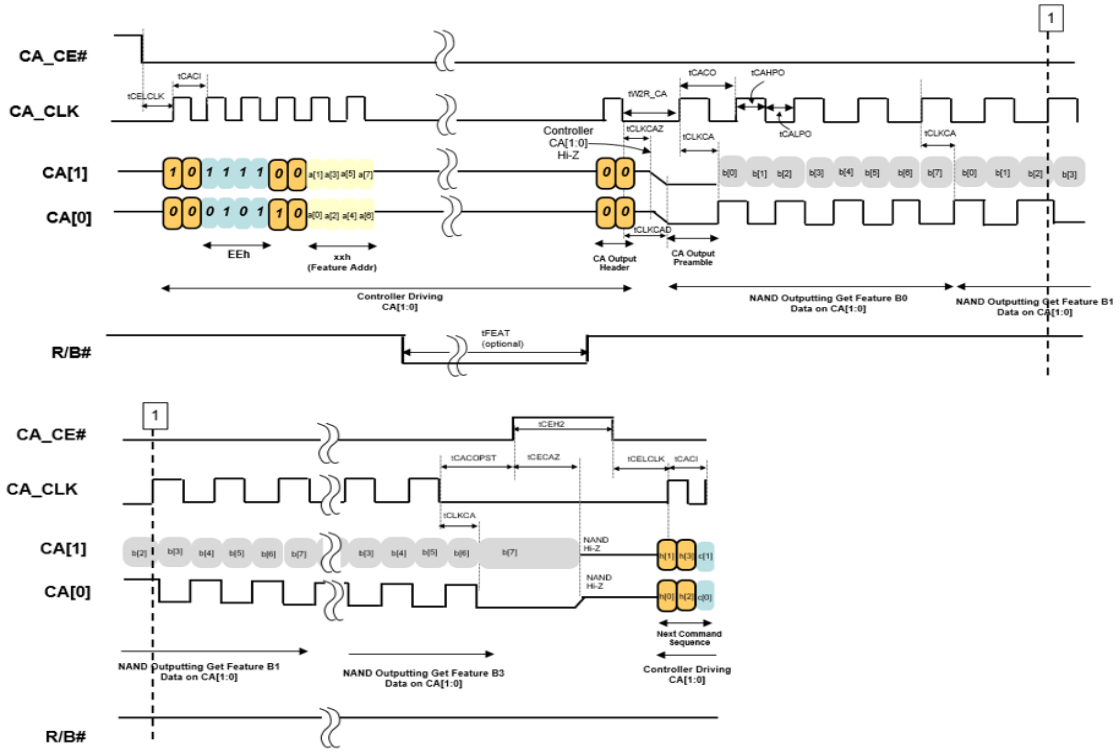


Figure 5-8 Get Feature (EEh) with Multi-Byte CA Output Packet Format

Thus, for command sequences with multiple bytes of CA bus output from the NAND (i.e. Get Feature, Get Feature by LUN, Read ID), the multi-byte CA output packet format is more efficient versus the single-byte CA output packet format. However, for command sequences that produce only one byte of output from the NAND (ie. Read Status), single-byte and multi-byte CA output format bus efficiencies are the same.

Similar to the single-byte CA output case, CA output mode is entered via CA Data Output header and CA output mode is exited by bringing CA_CE# high.

5.7.4. Additional CA[1:0] Output Timing Specifications

The figure below shows additional CA[1:0] timing specifications during the CA output burst. These timings specifications are applicable for both single-byte and multi-byte CA output packet formats:

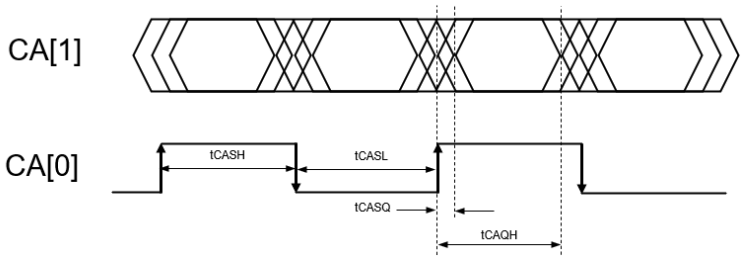


Figure 5-9 Additional CA[1:0] Output Timing Specifications

5.8. SCA Header Definition

The table below shows the different SCA headers and corresponding packet types currently defined in the SCA protocol:

Header rising edge		Header falling edge		CA Packet Type	CA Packet Structure
CA[1] (h[1]) (CLE)	CA[0] (h[0]) (ALE)	CA[1] (h[3]) (CLE)	CA[0] (h[2]) (ALE)		
0	0	0	0	CA Data Output	Output
0	0	0	1	VSP	VSP
0	0	1	0	CA Data Input	Input
0	0	1	1	VSP	VSP
0	1	0	0	Address	Input
0	1	0	1	Reserved	Reserved
0	1	1	0	Reserved	Reserved
0	1	1	1	Reserved	Reserved
1	0	0	0	Command	Input
1	0	0	1	VSP	VSP
1	0	1	0	VSP	VSP
1	0	1	1	Non-Target ODT (NTO)	Input
1	1	0	0	LUN Selection (LUNSel) (optional)	Input
1	1	0	1	Select Chip Enable (SCE)	Input
1	1	1	0	Select Chip Pause (SCP)	Input
1	1	1	1	Select Chip Terminate (SCT)	Input

Table 5-3 SCA Header Definition Table

5.9. DQ Bus Control Packets

In the SCA protocol, DQ bus operations are controlled via Select Chip Enable (SCE), Select Chip Pause (SCP), Select Chip Terminate (SCT) and Non-Target ODT (NTO) packets.

5.9.1. Select Chip Enable (SCE) Packet

The Select Chip Enable (SCE) packet is used to start or resume a data burst on the DQ bus. The data burst is started or resumed on the addressed LUN on the CA_CE#.

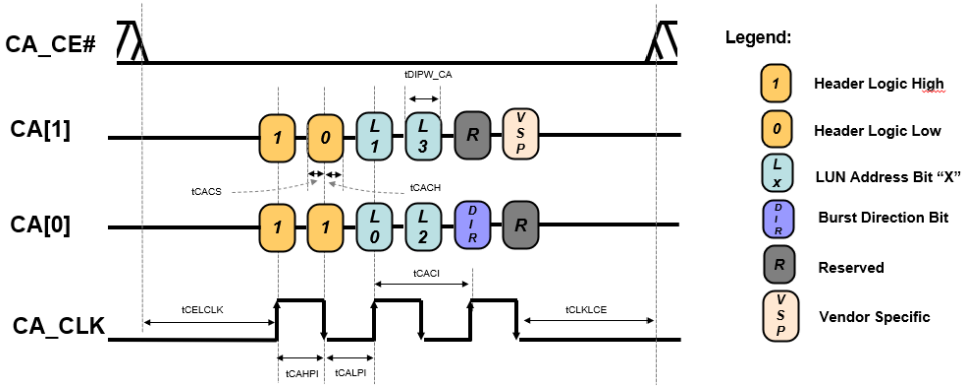


Figure 5-10 Select Chip Enable (SCE) Packet

The DIR (Burst Direction Bit) is required to be supported by the controller while it is optional to be supported by NAND devices. When the DQ bus burst enabled by the SCE packet is in the data input direction for the NAND, the controller shall input '1' on the DIR bit. When the burst enabled by the SCE packet is in the data output direction for the NAND, the controller shall input '0' on the DIR bit.

For each Reserved bit, the host shall input '0b'.

When DQ warmup cycles are enabled, DQ warmup cycles occur after any SCE packet issuance, regardless of whether the SCE is the first one for the data burst, or a succeeding one that resumes a paused data burst (data burst paused by a prior SCP packet).

5.9.2. Select Chip Pause (SCP) Packet

The Select Chip Pause (SCP) packet is used to pause an on-going data burst on the DQ bus. The data burst is paused on the addressed LUN on the CA_CE#. Once the data burst on a LUN has been paused, it may be resumed by the controller at a later time by issuing an SCE packet to the LUN.

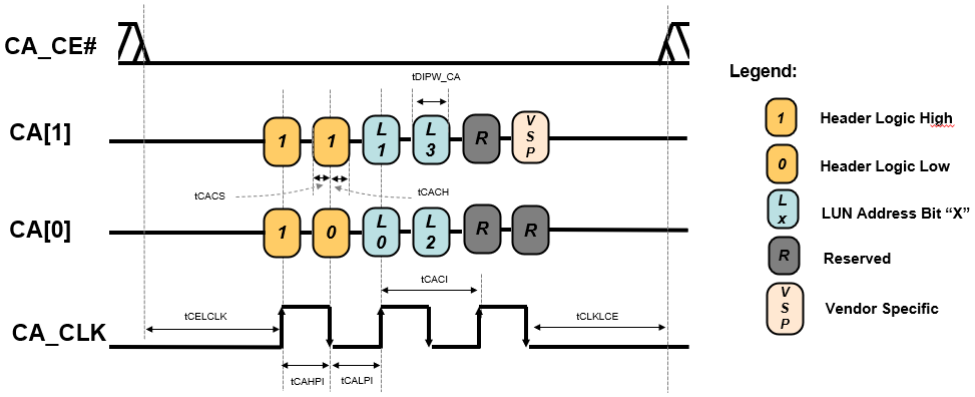
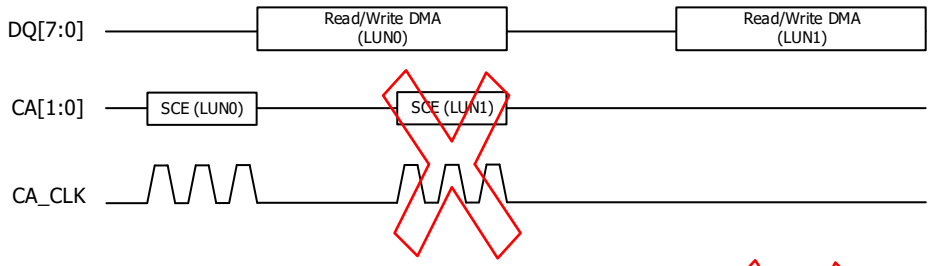


Figure 5-11 Select Chip Pause (SCP) Packet

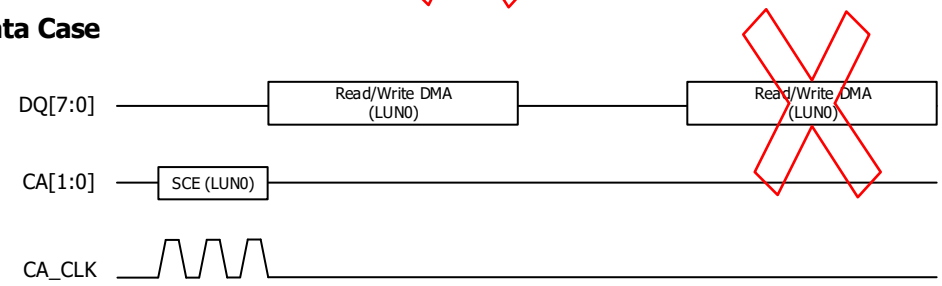
For each Reserved bit, the host shall input '0b'.

SCP packet is required when pausing data for both resume data burst on a LUN and start a data burst on other LUN. Consecutive issuance of SCE packet without SCP packet is not allowed.

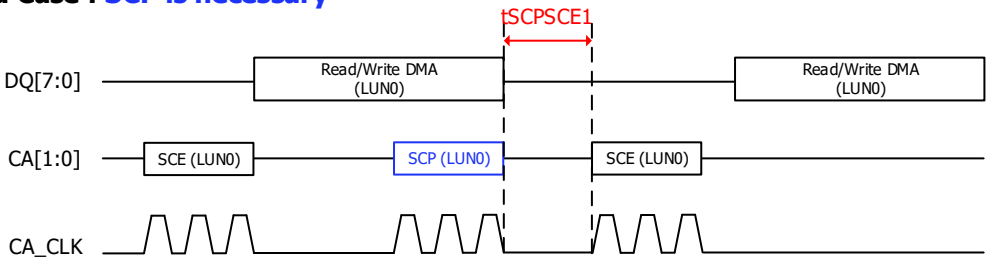
Pausing data + Interleaving Case



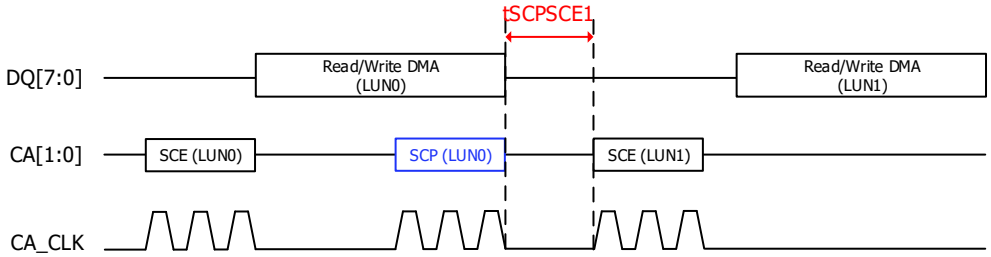
Pausing data Case



Pausing data Case : SCP is necessary



Pausing data + Interleaving Case [1]: SCP is needed



Note: 1) Supporting of Pausing data + Interleaving case is vendor specific and please follow each vendor's datasheet for more detail guidance.

Figure 5-12 Proper Sequence of SCE Packet issuance with SCP Packet

5.9.3. Select Chip Terminate (SCT) Packet

The Select Chip Terminate (SCT) packet is used to terminate an on-going data burst on the DQ bus. The data burst is terminated on the addressed LUN on the CA_CE#. Once the data burst on the LUN has been terminated, it cannot be resumed again by an SCE packet.

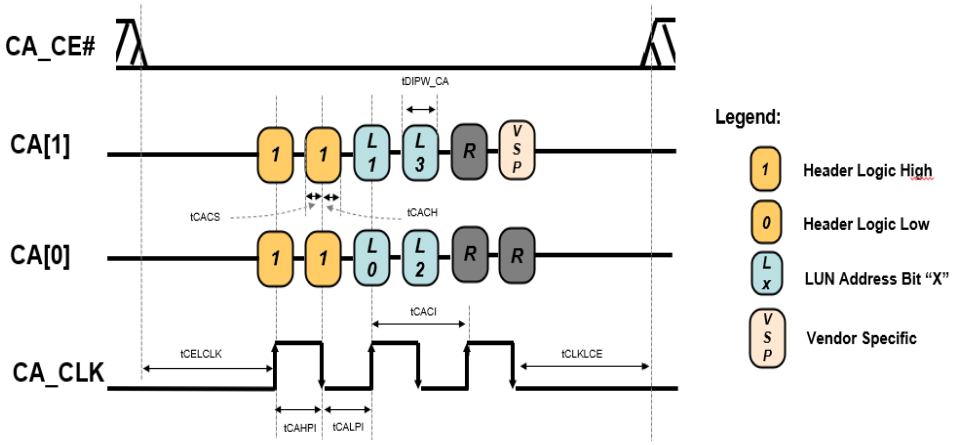


Figure 5-13 Select Chip Terminate (SCT) Packet

For each Reserved bit, the host shall input '0b'.

To terminate a paused data burst (data burst paused with the SCP packet), the data burst must be resumed first by an SCE packet prior to issuance of the SCT packet.

5.9.4. Data Input Burst Sequence

The SCE packet is used to start/resume a data input burst on the DQ bus, while SCP or SCT packets are used to pause or end a data input burst, respectively. The figure below shows a data input burst sequence on the DQ bus and some of the relevant timings related to the sequence:

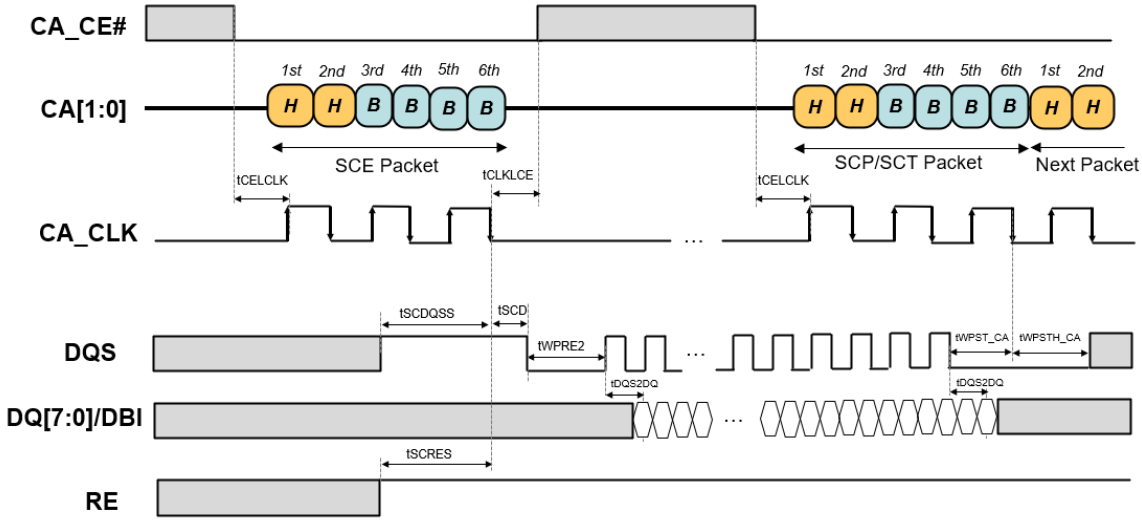


Figure 5-14 Data Input Burst Sequence

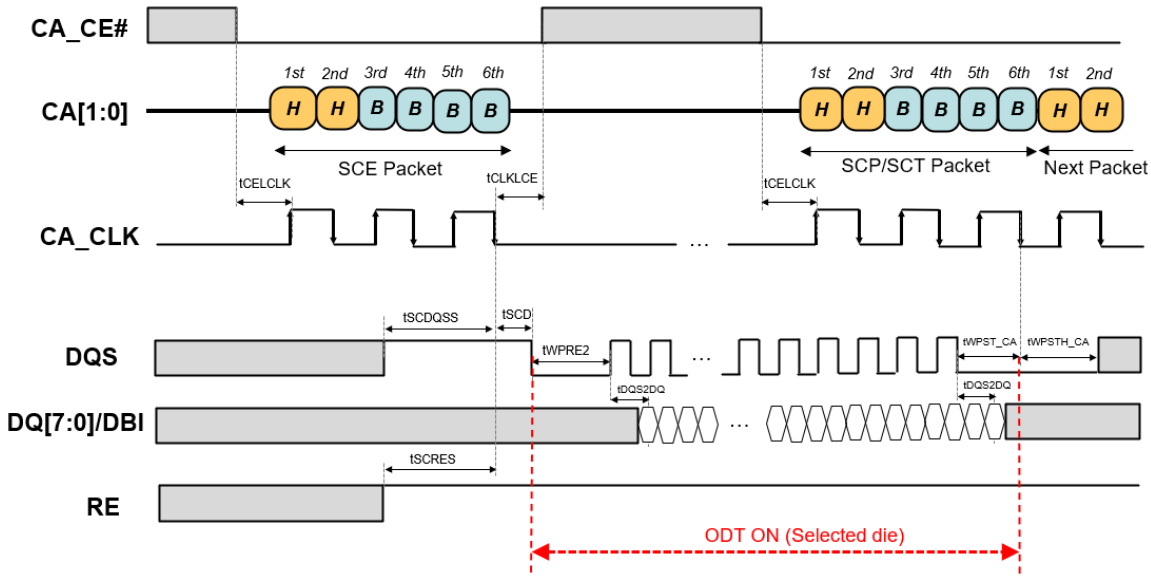


Figure 5-15 Data Input Burst Sequence with ODT (Self-Termination)

5.9.5. Data Output Burst Sequence

The SCE packet is used to start/resume a data output burst on the DQ bus, while SCP or SCT packets are used to pause or end a data output burst, respectively. The figure below shows a data output burst sequence on the DQ bus and some of the relevant timings related to the sequence:

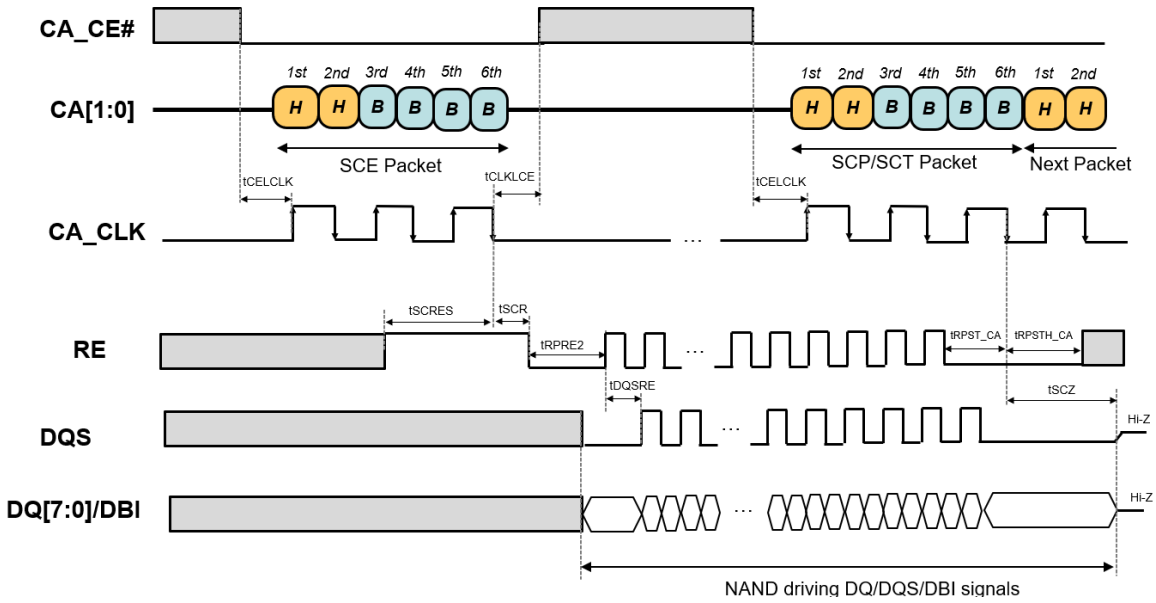


Figure 5-16 Data Output Burst Sequence

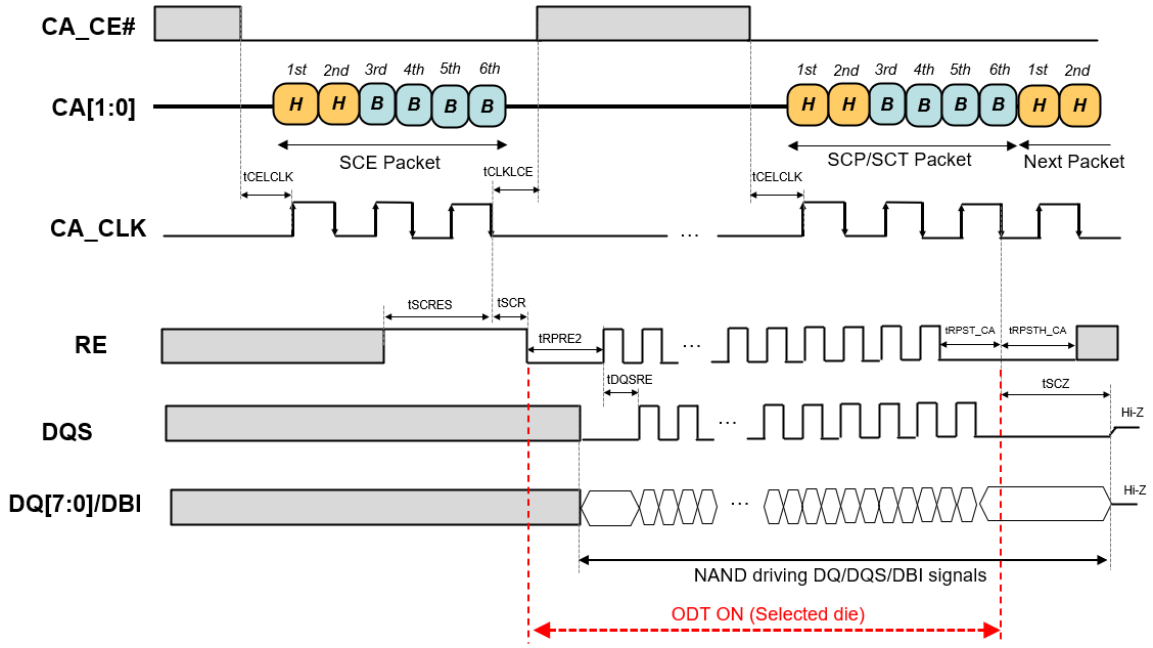


Figure 5-17 Data Output Burst Sequence with ODT (Self-Termination)

5.9.6. Data Output Sequence Restrictions

After the latency time associated with a LUN-level or plane-level NAND array read command (ie. tR), a Change Read Column Enhanced or Change Read Column (if supported by NAND vendor) command is required to be issued prior to the SCE command that enables the output of array data from the LUN.

The figure below shows the proper sequence where a Change Read Column Enhanced / Change Read Column (if supported by NAND vendor) command is issued after the array read latency time (ie. tR), prior to the SCE command:

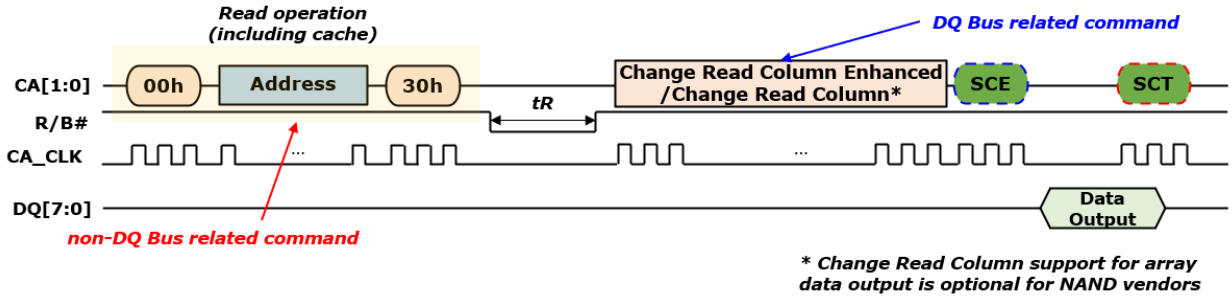


Figure 5-18 Proper Data Output Sequence

Note that for CE#-level array read commands (e.g. Read Parameter Page), NAND vendors may require the use of Change Read Column instead of Change Read Column Enhanced command after the end of the read latency time, prior to the SCE command for data output.

The figure below shows an example of an illegal data output sequence due to missing Change Read Column Enhanced / Change Read Column (if supported by NAND vendor) command between the end of read latency time (ie. tR) and the SCE command:

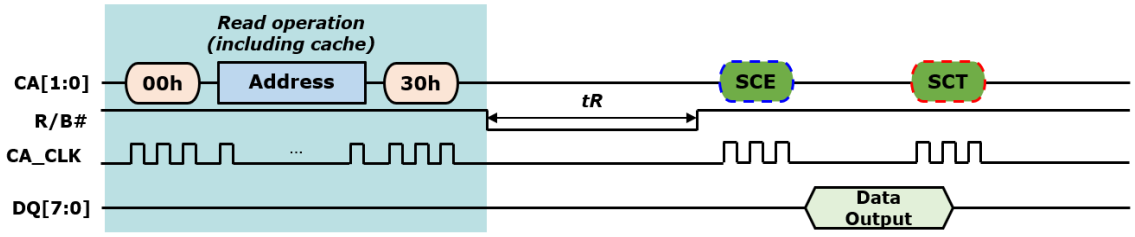


Figure 5-19 Illegal Data Output Sequence Due to Missing Change Read Column Enhanced / Change Read Column

Issuing a 00h command instead of Change Read Column Enhanced or Change Read Column (if supported by NAND vendor) command to enable output of array data is also not allowed. The figure below shows an example of an illegal data output sequence which uses 00h for array read data output:

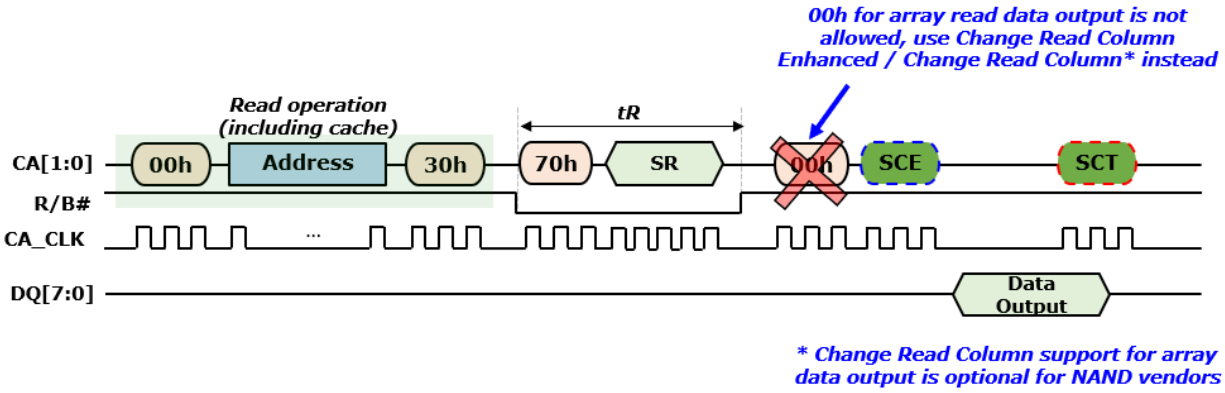


Figure 5-20 Illegal Data Output Sequence Due to Use of 00h Instead of Change Read Column Enhanced / Change Read Column

5.9.7. Non-Target ODT (NTO) Packet

The Non-Target ODT (NTO) packet is used to control non-target ODT operations on the DQ bus.

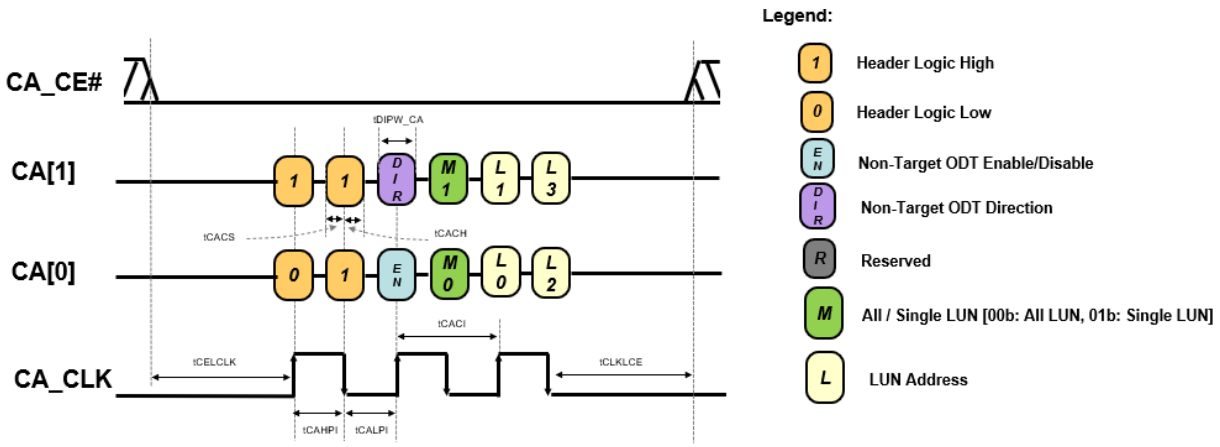


Figure 5-21 Non-Target ODT (NTO) Packet

To enable (assert) non-target ODT, the host shall input a '1' on the EN bit. To disable (de-assert) non-target ODT, the host shall input a '0' on the EN bit.

When EN = 1 and the Non-Target ODT Direction (DIR) bit is cleared to '0', non-target ODT for data output burst is enabled. When EN = 1 and the Non-Target ODT Direction (DIR) bit is set to '1', non-target ODT for data input burst is enabled.

The M[1:0] and L[3:0] bits are optional for NAND vendors to support but are required for controller vendors to support. When NAND devices in the system do not support M[1:0] and L[3:0] bit functionality, the host shall drive M[1:0] and L[3:0] bits LOW.

When M[1:0] and L[3:0] bits are supported by the NAND, and when M[1:0] = 00b, the NTO packet enables/disables non-target ODT on all LUNs on the CA_CE# that have been configured to provide non-target ODT (the NTO packet LUN address bits are ignored).

When M[1:0] and L[3:0] bits are supported by the NAND, and when M[1:0] = 01b, the NTO packet enables/disables non-target ODT on a specific LUN on the CA_CE#. The LUN address bits L[3:0] select which LUN on the CA_CE# responds to the NTO packet. The L[3:0] decoding is such that when L[3:0] = 0h, then LUN0 responds to the NTO packet, when L[3:0] = 1h, then LUN1 responds, when L[3:0] = 2h, then LUN2 responds, and so on.

The following figure is an example showing the use of NTO packets in asserting and de-asserting non-target ODT on a 4 package/4 CA_CE# channel system

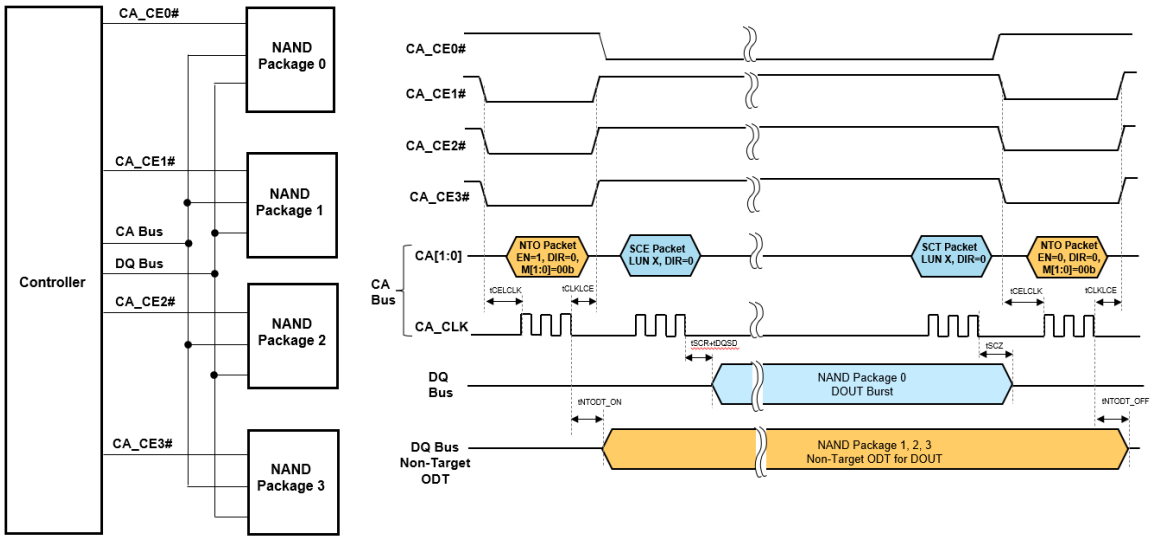


Figure 5-22 NTO Packet Usage All LUN in CA_CE# Example

As can be seen in the example above, in order to enable or disable non-target ODT on NAND Packages 1, 2 and 3 with a single NTO packet issuance, the CA_CE# signals for those packages are all asserted when the NTO packet is issued. In order to provide a constant non-target ODT value during the entire data burst, the NTO packets encapsulate the SCE/SCT packets. Also, in the example above, with M[1:0]=00b in the NTO packets, all LUNs on the CA_CE# that were asserted during the NTO packet issuance, and which were pre-configured to provide non-target ODT, respond to the NTO packet. Issuing an NTO packet with M[1:0]=00b (all LUN mode) to the die with the data burst is prohibited.

The following figure shows an example of the use of the single LUN option (M[1:0]=01b) to achieve LUN granularity in non-target ODT control. An NTO packet with M[1:0] = 00b is initially issued to CA_CE1# to enable non-target ODT on the LUNs on CA_CE1#. Afterwards, another NTO packet with M[1:0]=01b and L[3:0]=1h is issued to CA_CE0# to enable non-target ODT on CA_CE0# LUN1. After burst completion, the non-target ODT is then disabled on CA_CE0# LUN1 and on the LUNs on CA_CE1#. Issuing an NTO packet with M[1:0]=01b (single LUN mode) to the die with the data burst is prohibited

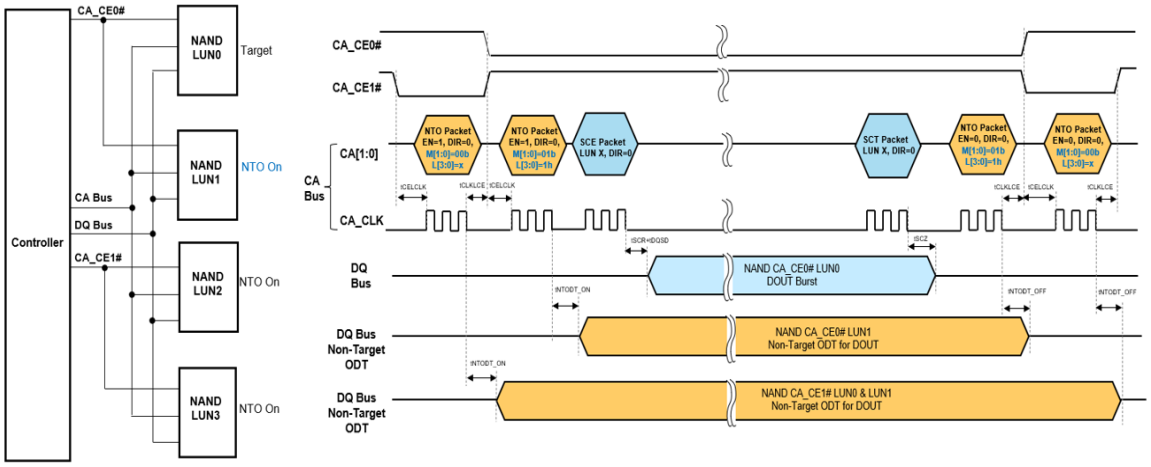


Figure 5-23 NTO Packet Usage with LUN Granularity Example

5.10. LUN Selection (LUNSel) Packet (Optional)

The LUN Selection (LUNSel) packet as showin in the figure below is used to give LUN context to subsequent commands, or to feedforward LUN/Plane information to improve subsequent command latencies. NAND vendor support for the LUNSel packet is optional.

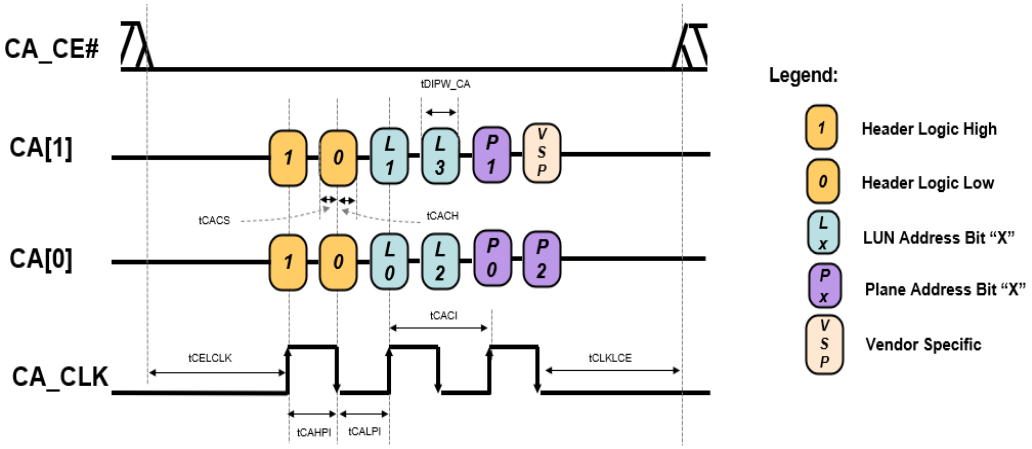


Figure 5-24 LUNSel Packet

After LUNSel packet issuance, the tLUNSEL_CA specification is required to be met prior to issuance of the next packet as shown in the figure below:

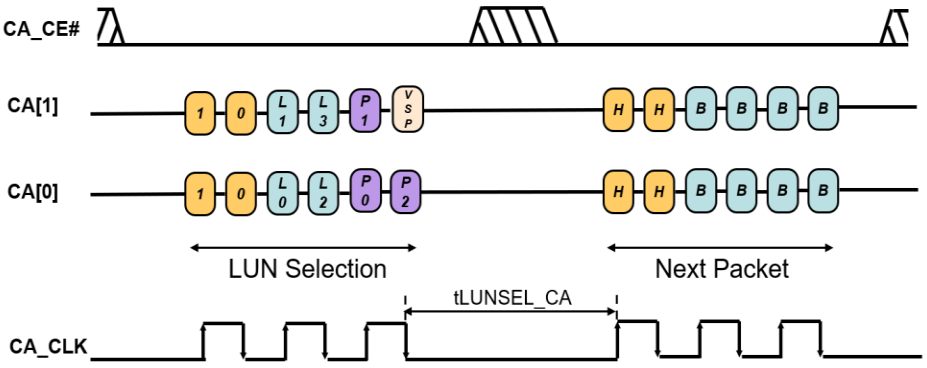


Figure 5-25 tLUNSEL_CA Requirement

The figure below shows optional use of the LUNSel packet in a program sequence to give LUN address context to the subsequent program confirm (10h) command. The figure also shows optional use of the LUNSel packet in front of the Program Page (80h) and Change Read Column (06h-E0h) command sequences to feedforward the LUN/plane address and improve latencies related to these command sequences.

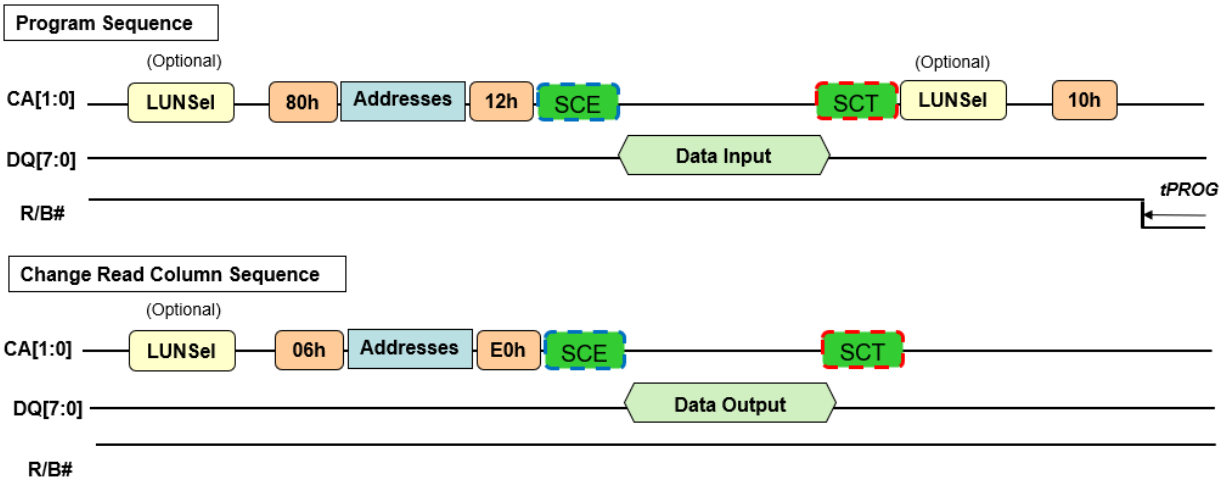


Figure 5-26 LUNSel Packet Usage

NAND vendors may support all or a subset of these optional LUNSel packet usages (see vendor datasheet).

5.11. Command Pointer Reset Sequence

The command pointer reset sequence allows the host to abort an on-going CA bus packet transaction on a CA_CE# by bringing CA_CE# high. When CA_CE# is brought HIGH in the middle of a packet transaction, the packet transaction is aborted and the LUNs on the CA_CE# restart their command pointers. The host must then restart packet transactions to the LUNs on the CA_CE#, beginning with header cycle input of the next packet:

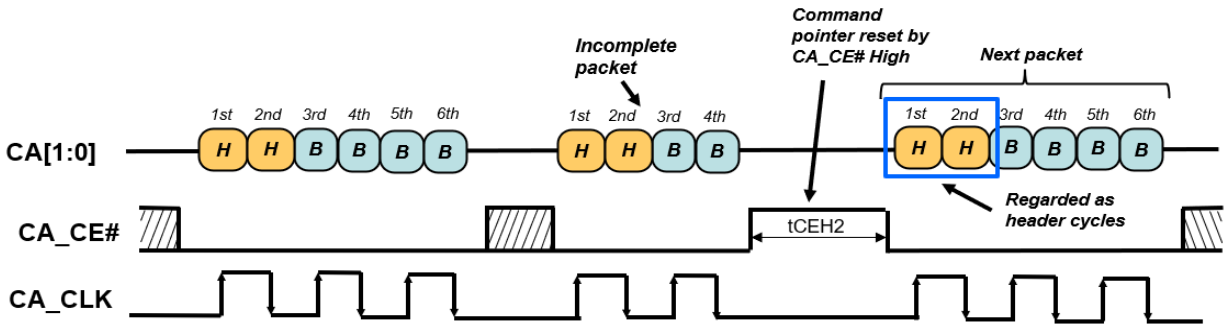


Figure 5-27 Command Pointer Reset Sequence

5.12. Miscellaneous Command Sequences

5.12.1. Set Feature Sequence

The figure below shows the SCA protocol Set Feature (EFh) sequence:

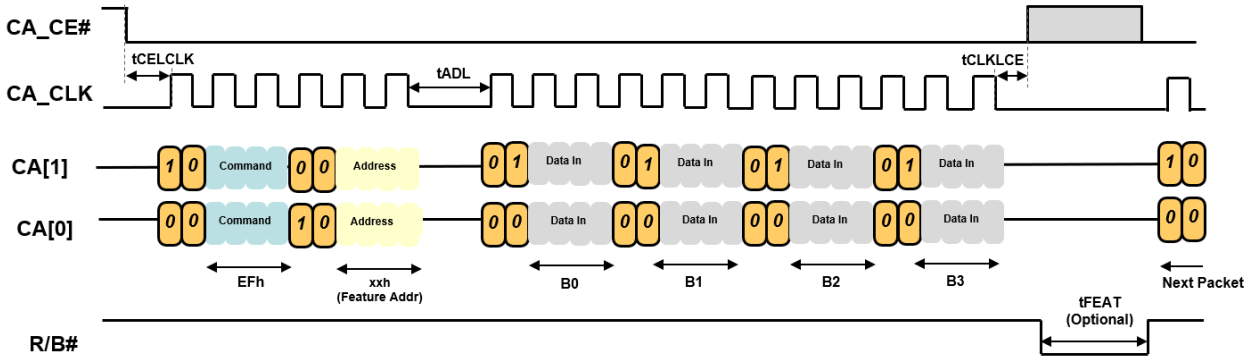


Figure 5-28 Set Feature (EFh) Sequence

5.12.2. Program Sequence

The following figure shows program sequences for both Conventional and SCA protocols:

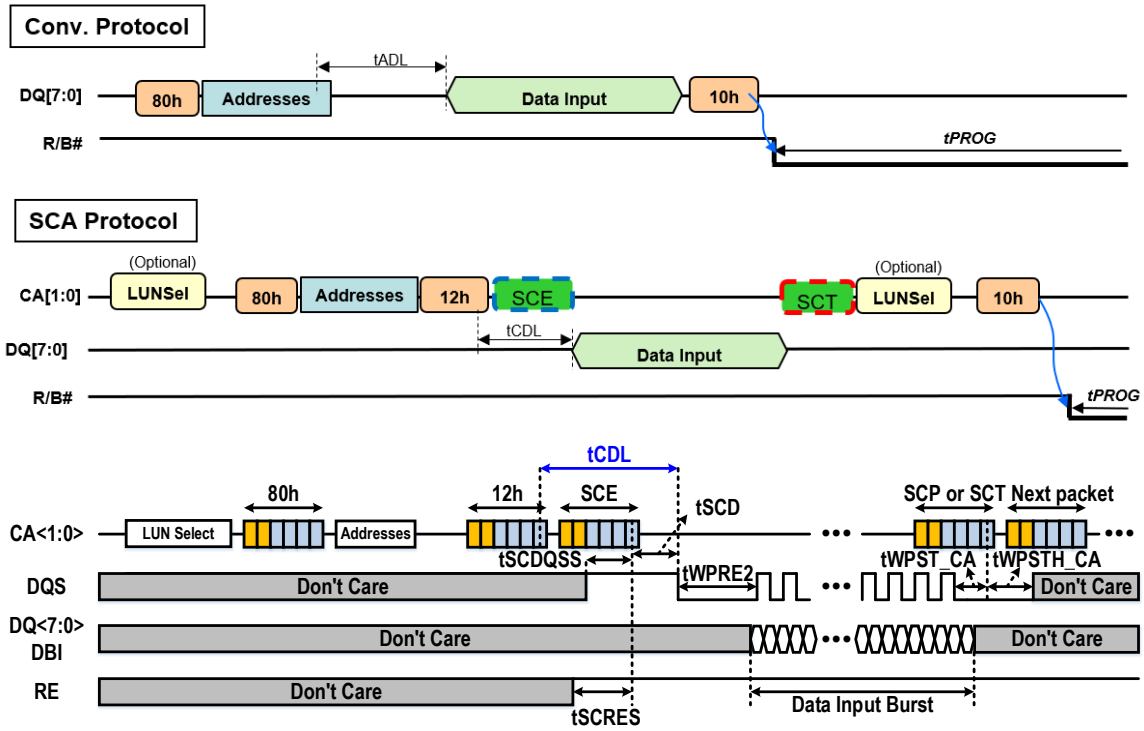


Figure 5-29 Conventional and SCA Protocol Program Sequences

The SCA protocol program sequence requires the use of a 12h command packet after address input. It also requires the use of SCE/SCP/SCT packets for the data input burst and the optional LUNSel packet may be required (see NAND vendor datasheet) prior to the 80h command packet and/or prior to the program execution command packet (ie. 10h).

5.12.3. Read Status Enhanced Sequence

The figure below shows the SCA protocol Read Status Enhanced (78h) sequence:

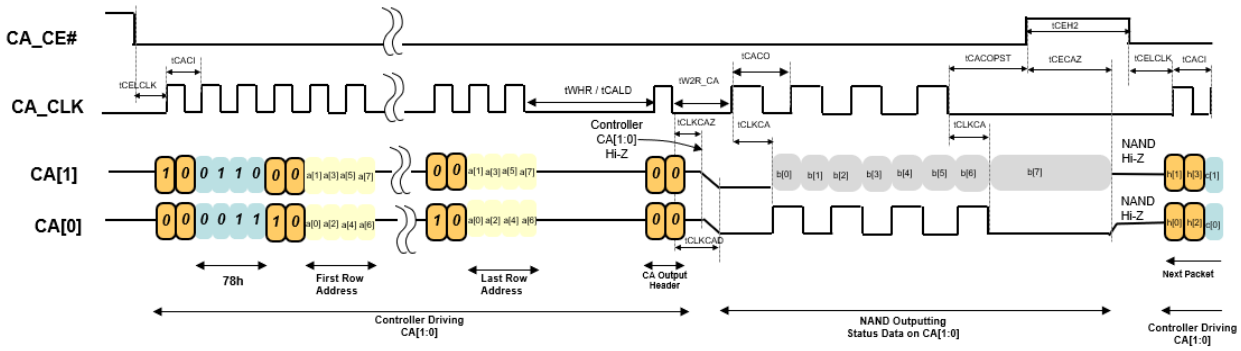


Figure 5-30 Read Status Enhanced (78h) Sequence

5.12.4. Change Read Column / Change Read Column Enhanced Sequence

The figure below shows the start of a Change Read Column / Change Read Column Enhanced sequence on a CA_CE# with 2 LUNs:

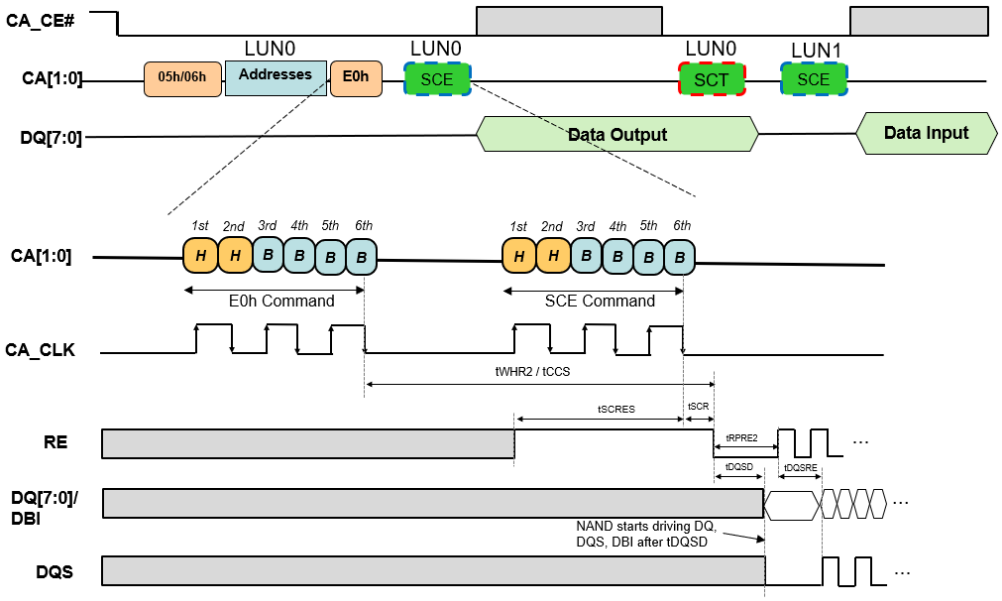


Figure 5-31 Start of Change Read Column / Change Read Column Enhanced Sequence

The figure below shows the end of the Change Read Column / Change Read Column Enhanced sequence on LUN0, back-to-back with an SCE packet that starts a data input burst on LUN1:

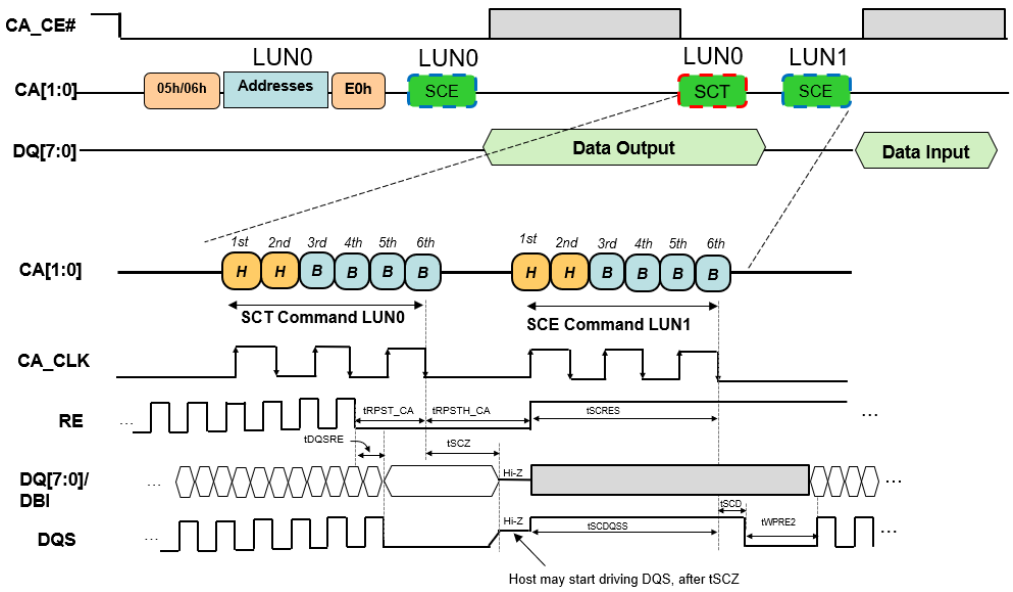


Figure 5-32 End of Change Read Column / Change Read Column Enhanced Sequence

5.12.5. Multi-Plane Program Sequence

The figure below shows the SCA Protocol Multi-Plane Program Sequence format:

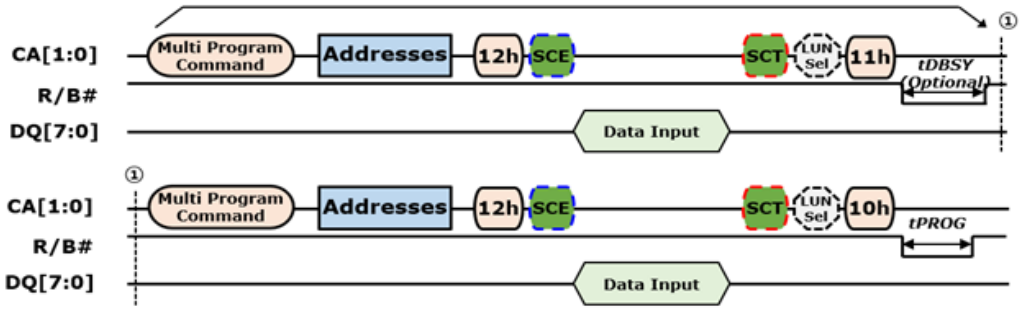


Figure 5-33 SCA Multi-Plane Program Sequence

Notes:

1) The figure above shows the command sequence for the last page in a multi-plane program sequence
2) Number of address cycles may vary across NAND vendors
3) Different program/confirm command op-codes may be supported by NAND vendors (see vendor datasheet)
4) The tDBSY busy time may also be optional (see vendor datasheet)

The figure below shows an example of an allowed sequence where a command sequence to a different LUN (LUN Y) is interleaved while a data input burst is paused on a LUN (LUN X):

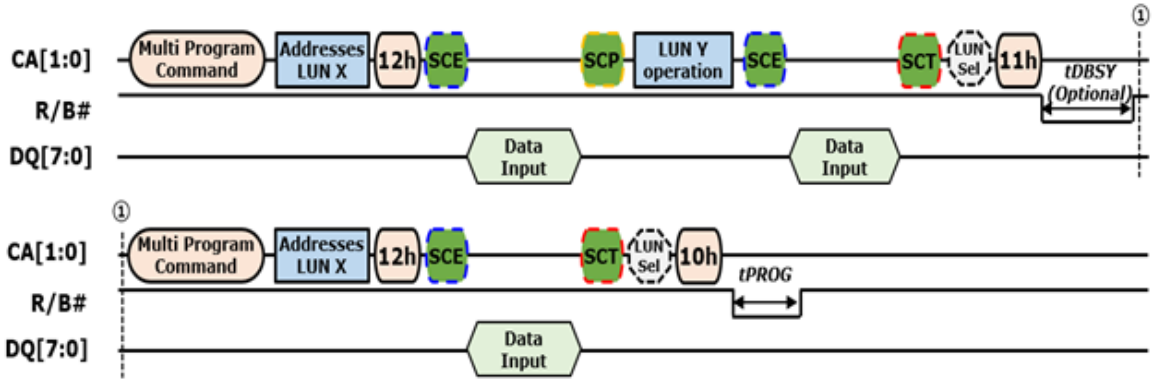


Figure 5-34 Example of Allowed SCA Multi-Plane Program Sequence With LUN Interleaving During Data Input Burst Pause

Notes:

1) Pausing the data burst is not needed when interleaving commands to another LUN. The example above just shows it is possible to interleave commands to another LUN after issuing an SCP to a LUN.

The figure below shows an example of sequences that are not allowed while there is a paused data input burst on a LUN:

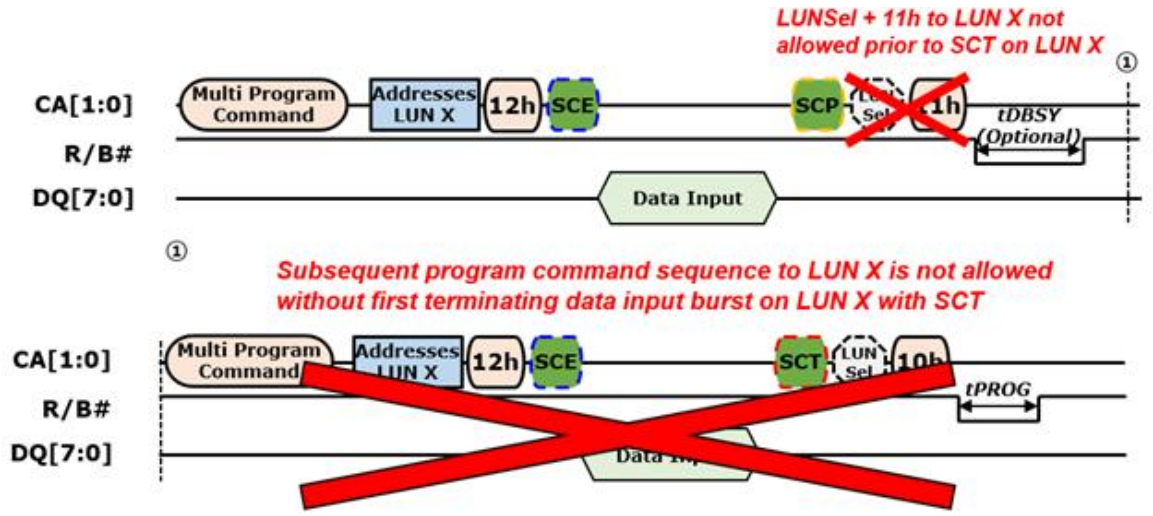


Figure 5-35 Example of Sequences Not Allowed when a LUN has Paused Data Input Burst

5.12.6. Multi-Plane Program Sequence with Change Row Address

The figure below shows the format for an SCA Protocol Multi-Plane Program Sequence with Change Row Address:

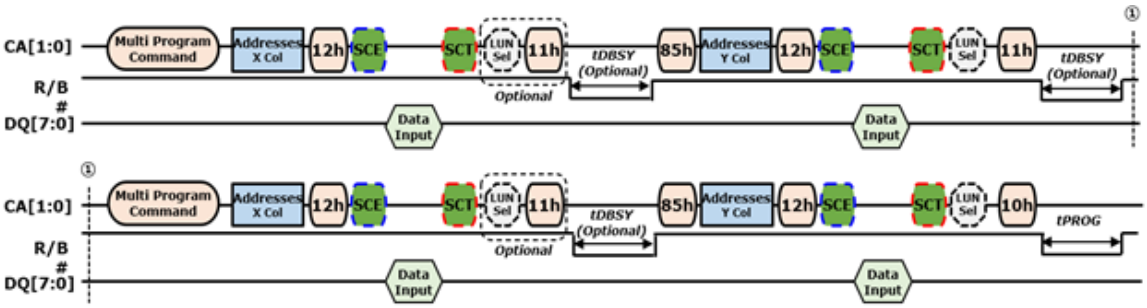


Figure 5-36 SCA Multi-Plane Program Sequence with Change Row Address

Notes:

1) The figure above shows the command sequence for the last page in a multi-plane program sequence
2) Number of address cycles may vary across NAND vendors
3) Different program/confirm command op-codes may be supported by NAND vendors (see vendor datasheet)
4) The tDBSY busy time may also be optional (see vendor datasheet)
5) NAND vendors may optionally require a LUNSel-11h prior to the Change Row Address (85h-Addresses-12h) sequence (see vendor datasheet)

5.12.7. Multi-Plane Cache Program Sequence

The figure below shows the SCA Multi-Plane Cache Program Sequence format:

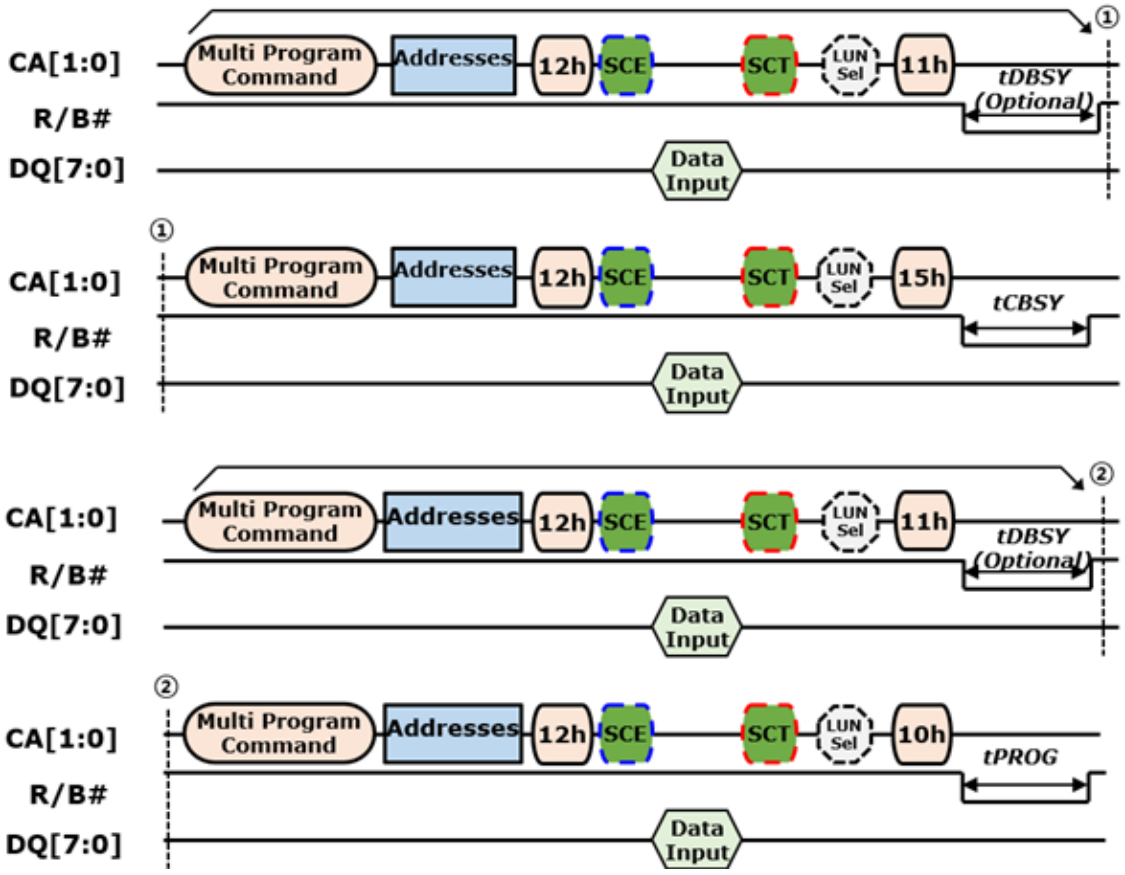


Figure 5-37 SCA Multi-Plane Cache Program Sequence

Notes:

1) The figure above shows the command sequence for the last 2 pages in a multi-plane cache program sequence
2) Number of address cycles may vary across NAND vendors
3) Different program/cache confirm command op-codes may be supported by NAND vendors (see vendor datasheet)
4) The tDBSY busy time may also be optional (see vendor datasheet)

5.13. Command Interleaving

5.13.1. DQ and Non-DQ Related Commands

Commands to the NAND may be classified into 2:

a) DQ related commands
b) Non-DQ related commands

DQ related commands are not allowed to be issued to a die that is still executing a prior DQ related command, has a paused data burst (by SCP command), or already has a queued up DQ related command awaiting data burst execution.

Non-DQ related commands may be issued to a die that is still executing a prior DQ related command, or already has a queued up DQ related command awaiting data burst execution (subject to NAND vendor specific restrictions).

The table below lists examples of DQ bus related and non-DQ bus related commands:

DQ Bus Related Commands	Non-DQ Bus Related Commands
Reads from NAND Cache Register / Page Register	Read Status Commands
Writes to NAND Cache Register / Page Register	Set Feature / Set Feature by LUN (1)
NAND Column Address Change Commands	Get Feature / Get Feature by LUN
Program Commands	Read ID
Erase Commands	Resets
DCC training via 18h command / Read DQ Training (62h) / Write DQ Training (63h/64h)	Array Read (with NAND vendor specific restrictions)

NOTE:
1. Set Feature / Set Feature by LUN sequences which change DQ bus input/output options (e.g. warmup cycles, ODT or other DQ bus settings) are prohibited to be issued to LUNs that have on-going DQ bus input/output operations or actively providing ODT on the channel.

Table 5-4 Examples of DQ Bus and Non-DQ Bus related commands

5.14. Command Interleaving Examples

The figure below illustrates improper interleaving of DQ related commands on a CA_CE# with 2 LUNs:

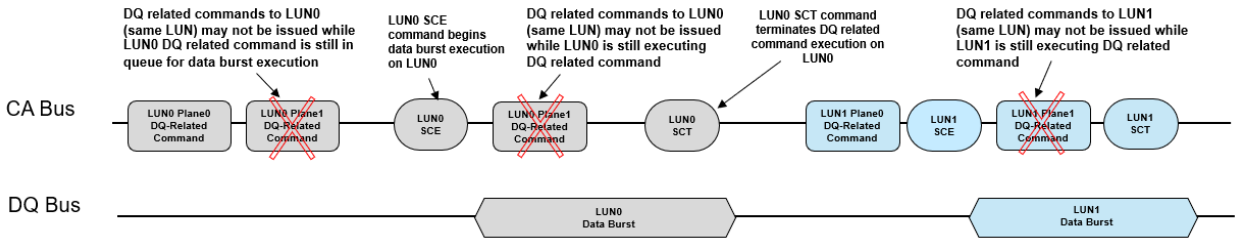


Figure 5-38 Improper DQ Related Command LUN Interleaving Example

The figure below illustrates proper interleaving of DQ related commands on a CA_CE# with 2 LUNs:

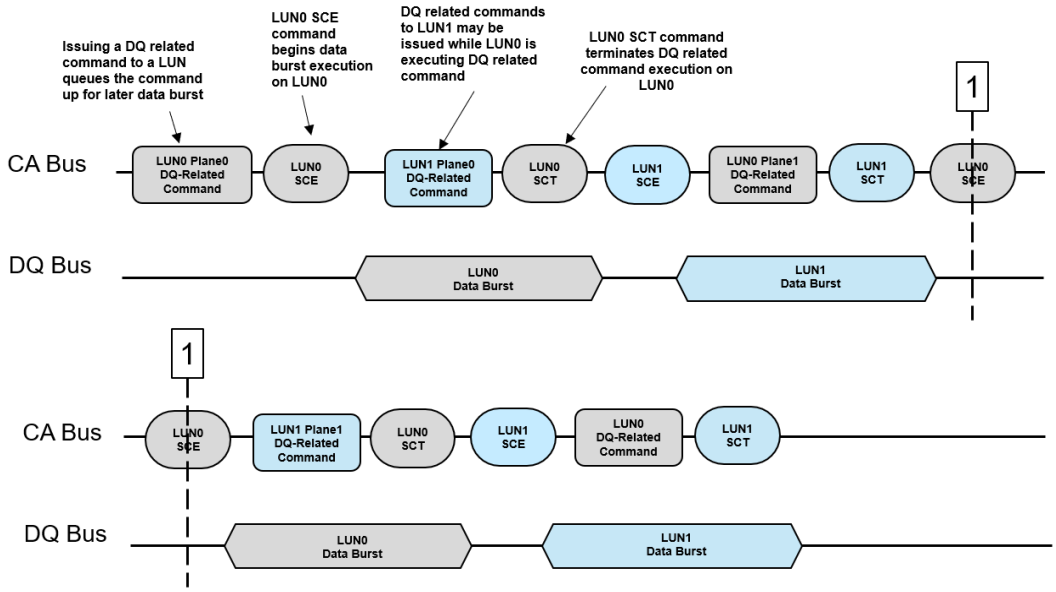


Figure 5-39 Proper DQ Related Command LUN Interleaving Example – Single CA_CE#

The figure below shows another example of proper LUN interleaving this time on a channel with multiple CA_CE#'s and multiple LUNs per CA_CE#:

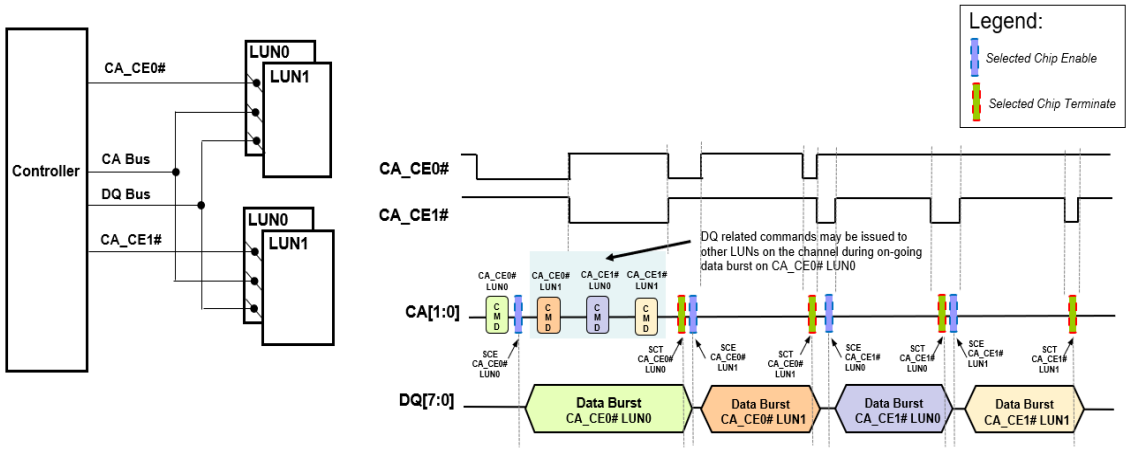


Figure 5-40 Proper DQ Related Command LUN Interleaving Example - Multiple CA_CE#

The figure below shows an example of proper interleaving of non-DQ related commands with DQ related commands on a CA_CE# with at least 3 LUNs:

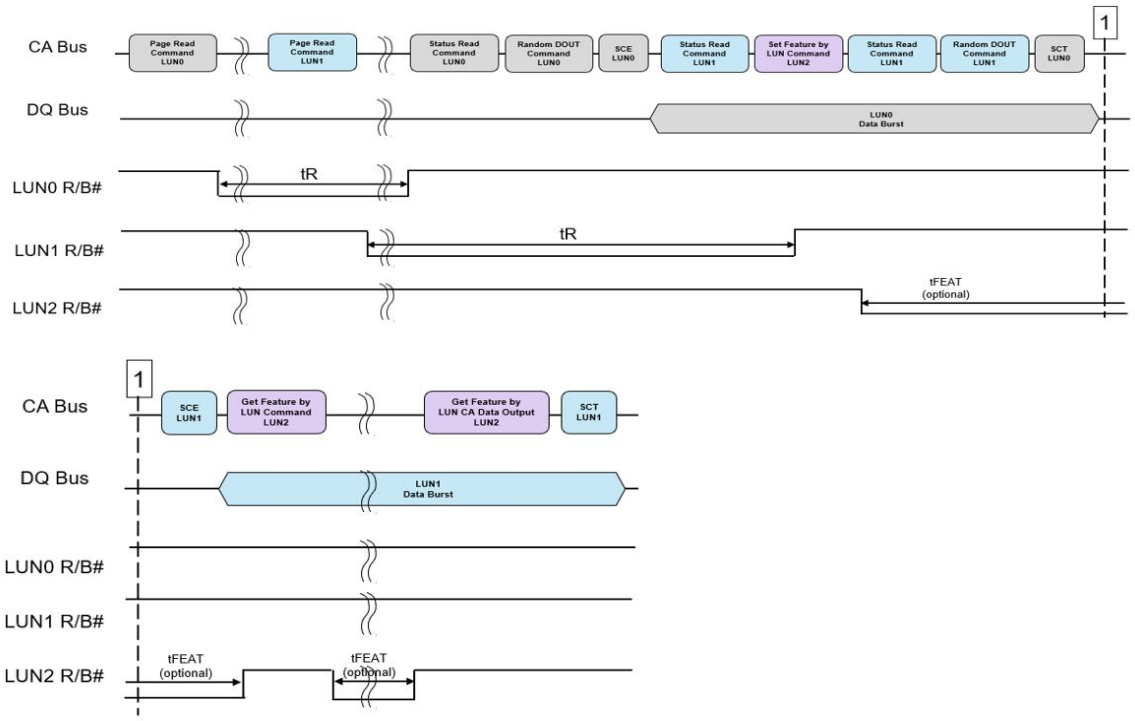


Figure 5-41 Proper DQ and Non-DQ Related Command LUN Interleaving Example

5.14.1. Status Reads / LUN Interleaving During Get Feature / Get Feature by LUN

Status Reads during Get Feature / Get Feature by LUN tFEAT are subject to NAND vendor specific restrictions (see NAND vendor device datasheet).

Status Reads or LUN interleaving during Get Feature / Get Feature by LUN sequences that do not have any busy time, are not allowed.

For Get Feature / Get Feature by LUN sequences that have a busy time, the following sequence to retrieve Get Feature / Get Feature by LUN data after Status Reads to same LUN may be supported.

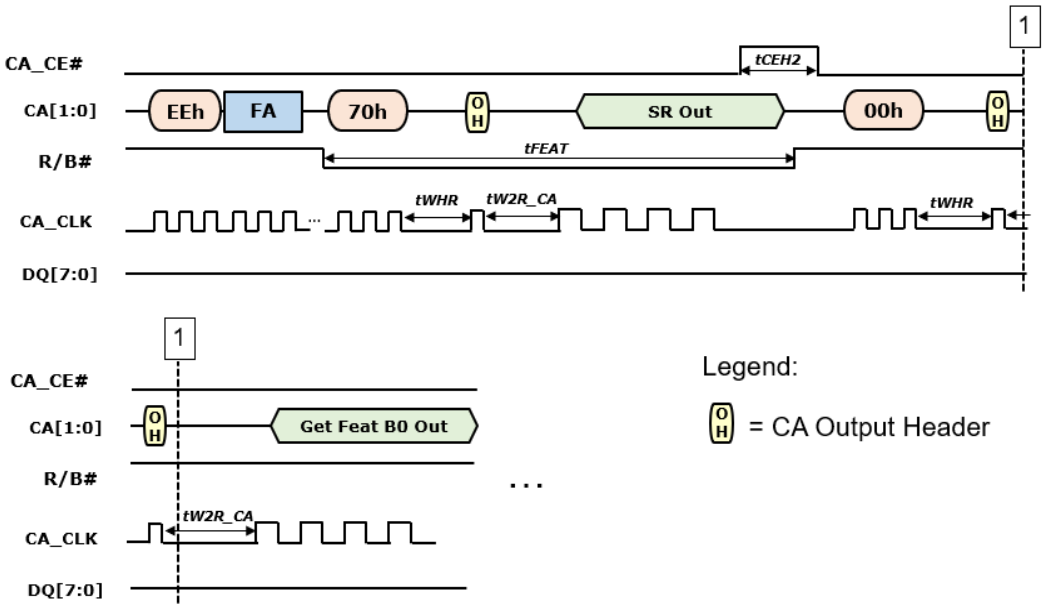


Figure 5-42 Get Feature Data Retrieval after Read Status to Same LUN

For Get Feature / Get Feature by LUN sequences that have a busy time, the following sequence to retrieve Get Feature / Get Feature by LUN data after LUN Interleaving may be supported.

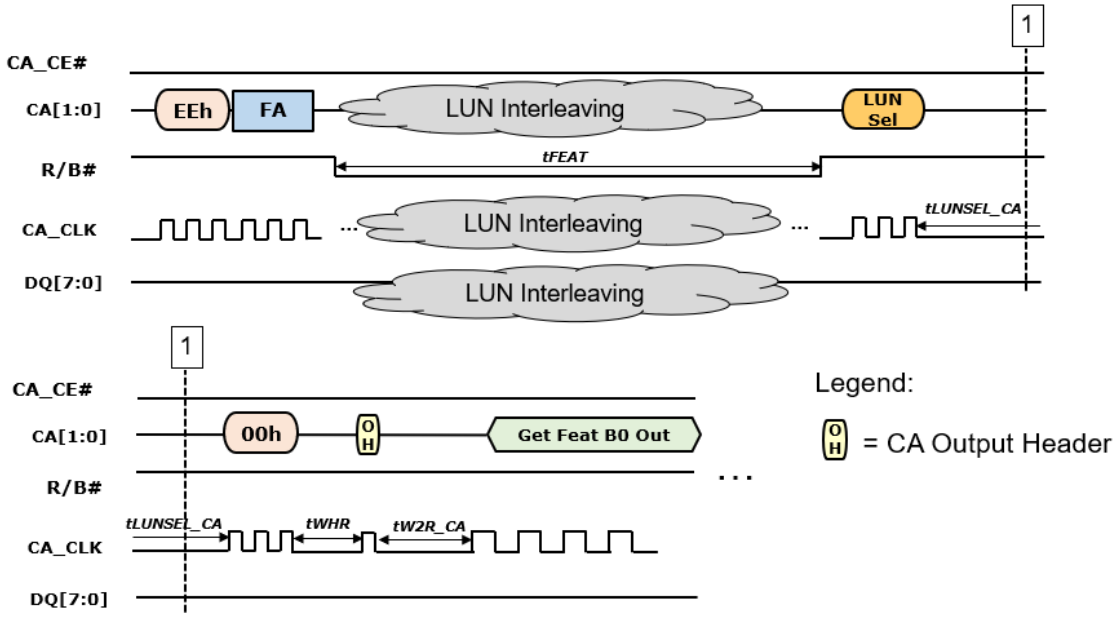


Figure 5-43 Get Feature Data Retrieval after LUN Interleaving

5.15. CA Training Feature Address Register (FA 25h) (Optional)

The FA 25h register can optionally be implemented by NAND vendors to provide a mechanism for the controller to train the CA bus. The host may write a data pattern to FA 25h (via Set Feature or Set Feature by LUN sequence) and read the written data pattern back out (via Get Feature or Get Feature by LUN sequence). The register bits in FA 25h do not affect any NAND functionality and the sole purpose is for CA bus training.

Sub-feature Parameter	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
B0	B0 data pattern							
B1	B1 data pattern							
B2	B2 data pattern							
B3	B3 data pattern							

Table 5-5 Feature Table for SCA Protocol CA Bus Training Register [25h]

5.16. SCA DQ Mirror Mode Bit (optional)

NAND devices may optionally support the SCA_DQMIRR bit at FA 02h P4[1]. In the SCA protocol, since the CA bus is separate from the DQ bus, it allows DQ mirror mode to be configured via Set Feature sequence on the CA bus.

When SCA_DQMIRR = ‘0’, then the DQ mirror function is disabled on the NAND. If SCA_DQMIRR = ‘1’, then the DQ mirror function is enabled on the NAND.

When the DQ mirror function is enabled, DQ[0] is logically interpreted by the NAND as DQ[7], DQ[1] as DQ[6], DQ[2] as DQ[5], DQ[3] as DQ[4], DQ[4] as DQ[3], DQ[5] as DQ[2], DQ[6] as DQ[1] and DQ[7] as DQ[0].

5.17. SCA Electrical Specifications – DC/AC Characteristics and Operating Conditions

5.17.1. SCA Protocol AC and DC Operating Conditions

The table below defines the AC/DC Operating conditions for the SCA Protocol Pins:

Category	Spec	Min	Max	Unit
CA Input Specs	V_{IH}.CA(AC)	0.8*VccQ	-	V
	V_{IH}.CA(DC)	0.7*VccQ	-	
	V_{IL}.CA(AC)	-	0.2*VccQ	
	V_{IL}.CA(DC)	-	0.3*VccQ	
CA Output Specs	VOH.CA(DC)	0.7*VccQ	-	
	VOL.CA(DC)	-	0.3*VccQ	
NOTE: 1. CA Input Specs apply to CA[1:0], CA_CLK, CA_CE# signals and also to SCA signal when the SCA signal is driven and not floated. 2. CA Output Specs apply to CA[1:0] signals. The NAND CA[1:0] nominal output drive strength is 50Ω and does not support ZQ calibration. 3. CA[1:0], CA_CLK, CA_CE# will operate unterminated 4. All AC Timing measurements are with respect to 0.5*VccQ signal crossing				

Table 5-6 SCA Protocol AC and DC Operating Conditions

The table below defines the SCA CA pins output accuracy requirements:

R_{ON} = 50 Ohms					
Symbol	VOUT to VssQ	Maximum	Nominal	Minimum	Unit
R_SCA_CApulldown	0.2 x VccQ	90.0	50.0	24.0	Ohms
	0.5 x VccQ	90.0	50.0	26.0	Ohms
	0.8 x VccQ	122.0	50.0	26.0	Ohms
R_SCA_CApullup	0.2 x VccQ	122.0	50.0	26.0	Ohms
	0.5 x VccQ	90.0	50.0	26.0	Ohms
	0.8 x VccQ	90.0	50.0	24.0	Ohms
R_SCA_CApupd_mismatch	0.5 x VccQ	25.0	-	-25.0	Ohms
NOTE: 1. The R_SCA_CApulldown, R_SCA_CApullup and R_SCA_CApupd_mismatch specifications apply to CA[1:0] signals					

Table 5-7 SCA Protocol CA Pins Output Accuracy

The table below defines the SCA CA pins output leakage requirements:

Symbol	Description	Min	Max	Unit
ILOpd_SCA_CA	Output leakage current when SCA CA[1:0] are Hi-Z and VOUT = VccQ	-	20	uA
ILOpu_SCA_CA	Output leakage current when SCA CA[1:0] are Hi-Z and VOUT = VssQ	-	20	uA
NOTE: 1. The ILOpd_SCA_CA and ILOpu_SCA_CA specifications apply to CA[1:0] signals				

Table 5-8 SCA Protocol CA Pins Output Leakage

5.17.2. SCA Protocol AC Timings

The table below defines the AC Protocol Timings for the SCA Protocol Pins:

Symbol	Description	Min	Max	Unit	Notes
tCELCLK	CA_CE# setup to CA_CLK edge	20	-	ns	
tCLKLCE	CA_CLK# hold to CA_CE# edge	20	-	ns	
tCACI	CA_CLK input cycle time	4	-	ns	
tCAHPI	CA_CLK input cycle high time	0.45	-	tCACI	
tCALPI	CA_CLK input cycle low time	0.45	-	tCACI	
tCACS	CA setup time to CA_CLK @1V/ns slew rate	0.6	-	ns	
tCACH	CA hold time from CA_CLK @1V/ns slew rate	0.6	-	ns	
tCDL	The tCDL spec is the command-to-data loading time after the 12h command. Program/Change Row Address 12h command last CA_CLK edge to start of DIN burst (end of write pre-amble).	400	-	ns	1
tCEH2	Minimum CA_CE# high pulse width	30	-	ns	
tDIPW_CA	CA minimum input pulse width	0.33	-	tCACI	
tCACO	CA_CLK output cycle time	10	-	ns	
tCAHPO	CA_CLK output high time	0.45	-	tCACO	
tCALPO	CA_CLK output low time	0.45	-	tCACO	
tCLKCA	CA_CLK to CA output	-	30	ns	
tCACOPST	CA_CLK post-amble time	tCLKCA+0.5*tCACO	-	ns	
tCECAZ	CA_CE# high to CA Hi-Z time	0	30	ns	
tCASQ	CA to CA strobe skew	-	0.15*tCACO	ns	
tCAQH	CA hold time	Min(tCAHPO, tCALPO) – 0.15*tCACO	-	ns	
tCASH	CA strobe high time	tCAHPO – 0.15*tCACO	-	ns	
tCASL	CA strobe low time	tCALPO – 0.15*tCACO	-	ns	

tSCPSCE1	SCP to SCE restriction	VSP	-	ns	
tSCRES	RE_n valid before SCE command final CA_CLK low	10	-	ns	
tSCR	CA_CLK final edge to RE_n low	50	-	ns	
tRPRE2	RE_n pre-amble time	30	-	ns	
tRPST_CA	RE_n post-amble setup w.r.t. final CA_CLK edge	tDQSRE+0.5*tRC	-	ns	
tRPSTH_CA	RE_n post-amble hold w.r.t. final CA_CLK edge	50	-	ns	
tCLKCAD	CA output header last CA_CLK edge to CA output drive	-	20	ns	
tCLKCAZ	CA output header last CA_CLK edge to host Hi-Z (Note: Bus conflict impact is minimized when tCLKCAZ is shorter than tCLKCAD)	-	5	ns	
tW2R_CA	CA output header last CA_CLK edge to first CA_CLK for CA output (does not include tWHR)	20	-	ns	
tSCDQSS	DQS high before SCE command ginal CA_CLK low	10	-	ns	
tSCD	SCE command final CA_CLK low to DQS low	50	-	ns	
tWLCEL_CA	CA_CLK low setup to first CE# low after SCA protocol has been enabled	100	-	ns	
tWPRE2	DQS pre-amble time during write operation	25	-	ns	
tWPST_CA	DQS post-amble setup time w.r.t. final CA_CLK edge	6.5	-	ns	
tWPSTH_CA	DQS post-amble hold time w.r.t. final CA_CLK edge	50	-	ns	
tR2W_CA	Last CA output CA_CLK falling edge to the CA_CLK rising edge which starts the next header	tCACOPST + tCEH2 + tCELCLK	-	ns	
tDQSRE	Data output RE_n to DQS latency	-	25	ns	
tNODT_ON	NTO packet last CA_CLK falling edge to when non-target ODT is enabled	-	60	ns	
tNODT_OFF	NTO packet last CA_CLK falling edge to when non-target ODT is disabled	-	60	ns	
tSCZ	SCT/SCP packet last CA_CLK falling edge to when DQ/DQS/DBI signals are Hi-Z	-	50	ns	
tLUNSEL_CA	LUNSel packet last CA_CLK falling edge to next packet first CA_CLK rising edge	20	-	ns	

Notes: 1) tCDL = tADL – 3*tCACI

Table 5-9 SCA Protocol AC Timings

5.17.3. SCA CA Slew Rate Derating

When the slew rate of CA_CLK or CA[1:0] signals are < 1V/ns, the tCACS and tCACH specs shall each be derated according to values in the table below:

		CA_CLK Input Slew Rate (V/ns)							
		1.0	**0.9**	**0.8**	**0.7**	**0.6**	**0.5**	**0.4**	**0.3**
CA[1] or CA[0] Input Slew Rate (V/ns)	**1.0**	0	28	63					
	0.9	28	56	91	136				
	0.8	63	91	126	171	231			
	0.7		136	171	216	276	360		
	0.6			231	276	336	420	546	
	0.5				360	420	504	630	840
	0.4					546	630	756	966
	0.3						840	966	1176
NOTE: 1. Derating Values are in picoseconds									

Table 5-10 SCA Protocol CA Slew Rate Derating

5.18. SCA Reset Restrictions

5.18.1. SCA Reset (EFh) Restrictions

1. If a data output burst is on-going from a LUN on a CA_CE# (RE is being toggled for data output), the host is required to hold the RE signals static (RE_t = 0, RE_c = 1) prior to issuing the Reset (FFh) command to the CA_CE#. Issuance of SCT or SCP are not required prior the Reset (FFh) command to the CA_CE#.

2. If a data input burst is on-going to a LUN on a CA_CE# (DQS is being toggled for data input), the host is required to hold the DQS signals static (DQS_t = 0, DQS_c = 1) prior to issuing the Reset (FF) command to the CA_CE#. Issuance of SCT or SCP are not required prior the Reset (FFh) command to the CA_CE#

3. To ensure that the NAND devices on the CA_CE# accept the Reset (FFh) command, a Command Pointer Reset sequence is required to be issued by the host prior to the issuance of the Reset (FFh) command.

5.18.2. SCA Reset by LUN (FAh) Restrictions

1. If a data output burst is on-going from a LUN on a CA_CE# (RE is being toggled for data output), the host is required to hold the RE signals static (RE_t = 0, RE_c = 1) prior to issuing the Reset by LUN (FAh) sequence to that LUN. Issuance of SCT or SCP are not required prior to the issuance of a Reset by LUN (FAh) sequence to that LUN.

2. If a data input burst is on-going to a LUN on a CA_CE# (DQS is being toggled for data input), the host is required to hold the DQS signals static (DQS_t = 0, DQS_c = 1) prior to issuing the Reset by LUN (FAh) sequence to that LUN. Issuance of SCT or SCP are not required prior to the issuance of a Reset by LUN (FAh) sequence to that LUN.

3. If a data input burst is on-going to a LUN or a data output burst is on-going from a LUN on a CA_CE#, a Reset by LUN (FAh) sequence may be issued to a different LUN on the CA_CE# without holding the data input burst or data output burst static, provided that either:
    a. The LUN to which the Reset by LUN (FAh) is issued is not providing non-target ODT for the LUN which has an on-going data burst, or
    b. The LUN to which the Reset by LUN (FAh) is issued is providing non-target ODT, and the non-target ODT is unaffected by the Reset by LUN (FAh) sequence.

4. To ensure that the Reset by LUN (FAh) command is accepted by the LUN address by the Reset by LUN (FAh) command, a Command Pointer Reset sequence is required to be issued by the host prior to the issuance of the Reset by LUN (FAh) command.

5.18.3. Reset Timing Diagrams

The following figure shows the required reset sequence and timings when a data output burst is interrupted by a Reset (FFh) command:

The timings in the figure below are applicable to the Reset by LUN (FAh) sequence as well, except that for Reset by LUN (FAh), the tRPST and tRPSTH specs are referenced to the last CA_CLK falling edge of the last address cycle in the Reset by LUN (FAh) sequence.

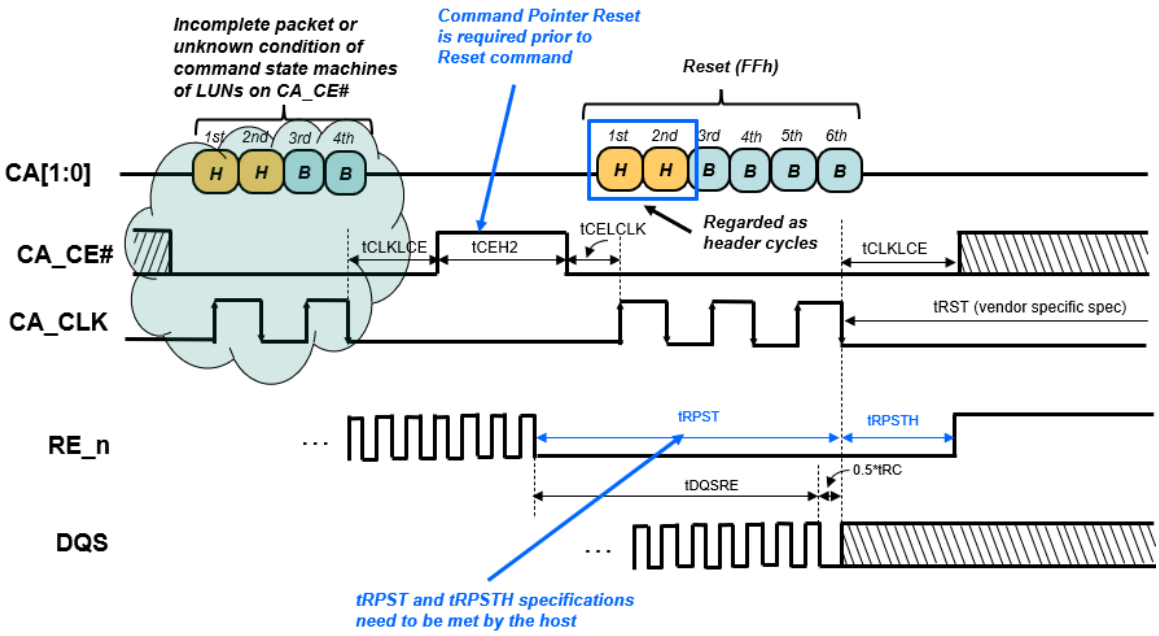


Figure 5-44 Data Output Burst Interrupted by Reset (FFh) Sequence

The figure below shows the required reset sequence and timings when a data input burst is interrupted by a Reset (FFh) command

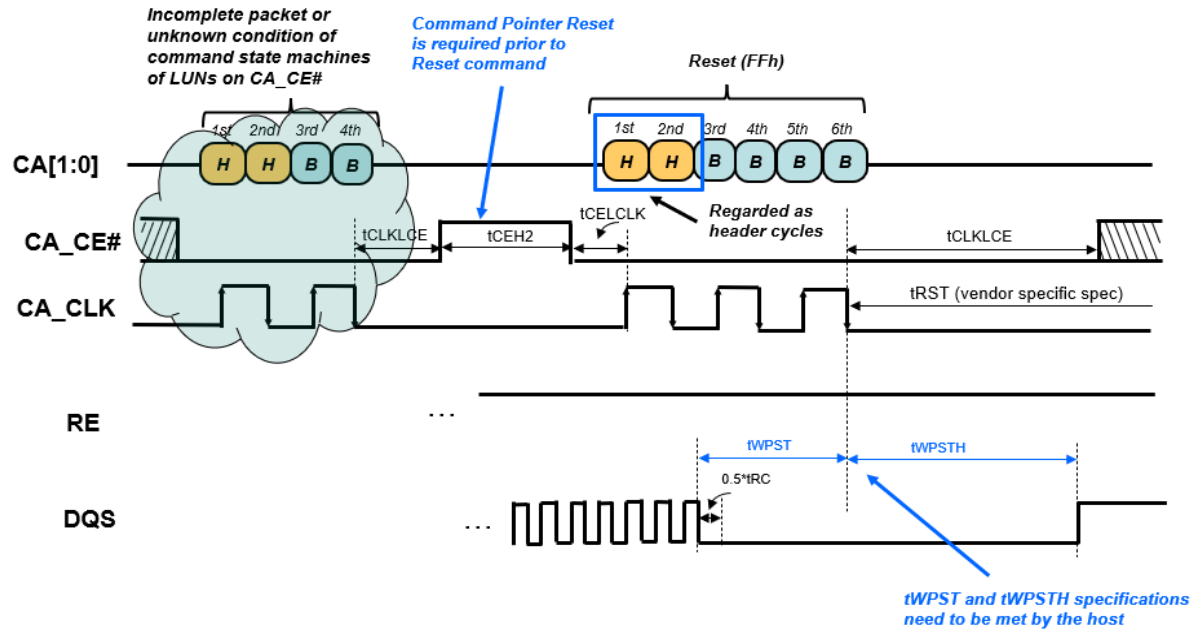


Figure 5-45 Data Input Burst Interrupted by Reset (FFh) Sequence

The timings in the figure above are applicable to the Reset by LUN (FAh) sequence as well, except that for Reset by LUN (FAh), the tWPST and tWPSTH specs are referenced to the last CA_CLK falling edge of the last address cycle in the Reset by LUN (FAh) sequence.

6. Command Definition

6.1. Command Sets

The following tables outline the ONFI command sets for the Conv. and SCA protocols. In the tables, the value specified in the first command cycle identifies the command to be performed. Some commands have a second command cycle. Typically, commands that have a second command cycle include address information in between.

Command	O/M	1st Cycle	2nd Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target level commands
Read	M	00h	30h		Y	
Multi-plane	O	00h	32h		Y	
Copyback Read	O	00h	35h		Y	
Change Read Column	O	05h	E0h		Y	
Change Read Column Enhanced	M	06h	E0h		Y	
Read Cache Random	O	00h	31h		Y	
ODT Disable	O	1Bh		Y	Y	Y
ODT Enable	O	1Ch		Y	Y	Y
Read Cache Sequential	O	31h			Y	
Read Cache End	O	3Fh			Y	
Block Erase	M	60h	D0h		Y	
Multi-plane	O	60h	D1h		Y	
Read Status	M	70h		Y	Y	
Read Status Enhanced	O	78h		Y	Y	
Page Program	M	80h	10h		Y	
Multi-plane	O	80h	11h		Y	
Page Cache Program	O	80h	15h		Y	
Copyback Program	O	85h	10h		Y	
Multi-plane	O	85h	11h		Y	
Small Data Move[2]	O	85h	11h		Y	
Change Write Column[1]	O	85h			Y	
Change Row Address[1]	M	85h			Y	
Read ID	M	90h				Y
Volume Select[3]	O	E1h		Y	Y	
ODT Configure[3]	O	E2h				
Read Parameter Page	M	ECh				Y
Read Unique ID	O	EDh				Y
Get Features	O	EEh				Y
Set Features	O	EFh				Y
Command Based DCC Training	O	18h				
Read DQ Training	M	62h				
Write TX DQ Training Pattern	M	63h				
Write TX DQ Training Readback	M	64h				
Write RX DQ Training	O	76h				
LUN Get Features	O	D4h			Y	
LUN Set Features	O	D5h			Y	
ZQ Calibration Short	O	D9h			Y	
ZQ Calibration Long	O	F9h			Y	
Reset LUN	O	FAh		Y	Y	
Synchronous Reset	O	FCh		Y	Y	Y
Reset	M	FFh		Y	Y	Y

NOTE:
1. Change Write Column specifies the column address only. Change Row Address specifies the row address and the column address. Refer to the specific command definitions. NAND vendors may support only Change Row Address, or both Change Row Address and Change Write Column command sequences.
2. Small Data Move's first opcode may be 80h if the operation is a program only with no data output. For the last cycle of a Small Data Move, it is a 10h command to confirm the Program or Copyback operation.
3. Volume Select shall be supported if the device supports either CE_n pin reduction or matrix termination. ODT Configure shall be supported if the device supports matrix termination.

Table 6-1 Conventional Protocol Command Set

Command Set Sequence	O/M	1st Command Packet	2nd Command Packet	3rd Command Packet	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target level commands
Read	M	00h	30h			Y	
Multi-plane	O	00h	32h			Y	
Copyback Read	O	00h	35h			Y	
Change Read Column	O	05h	E0h			Y	
Change Read Column Enhanced	M	06h	E0h			Y	
Read Cache Random	O	00h	31h			Y	
ODT Disable	O	1Bh			Y	Y	Y
ODT Enable	O	1Ch			Y	Y	Y
Read Cache Sequential	O	31h				Y	
Read Cache End	O	3Fh				Y	
Block Erase	M	60h	D0h			Y	
Multi-plane	O	60h	D1h			Y	
Read Status	M	70h			Y	Y	
Read Status Enhanced	O	78h			Y	Y	
Page Program	M	80h	12h	10h		Y	
Multi-plane	O	80h	12h	11h		Y	
Page Cache Program	O	80h	12h	15h		Y	
Copyback Program	O	85h	12h	10h		Y	
Multi-plane	O	85h	12h	11h		Y	
Small Data Move[2]	O	85h	12h	11h		Y	
Change Write Column[1]	O	85h	12h			Y	
Change Row Address[1]	M	85h	12h			Y	
Read ID	M	90h					Y
Read Parameter Page	M	ECh					Y
Read Unique ID	O	EDh					Y
Get Features	O	EEh					Y
Set Features	O	EFh					Y
Command Based DCC Training	O	18h					
Read DQ Training	M	62h					
Write TX DQ Training Pattern	M	63h					

Write TX DQ Training Readback	M	64h					
Write RX DQ Training	O	76h					
LUN Get Features	O	D4h				Y	
LUN Set Features	O	D5h				Y	
ZQ Calibration Short	O	D9h				Y	
ZQ Calibration Long	O	F9h				Y	
Reset LUN	O	FAh			Y	Y	
Synchronous Reset	O	FCh			Y	Y	Y
Reset	M	FFh			Y	Y	Y

NOTE:

1. Change Write Column specifies the column address only. Change Row Address specifies the row address and the column address. Refer to the specific command definitions. NAND vendors may support only Change Row Address, or both Change Row Address and Change Write Column command sequences.
2. Small Data Move's first opcode may be 80h if the operation is a program only with no data output. For the last command packet of a Small Data Move, it is a 10h command to confirm the Program or Copyback operation.
3. The command set above shall apply to command packets in the SCA protocol. Note that the SCA protocol has other packet types aside from command packets, see SCA section for description of other packet types.
4. Issuance of LUNSel, SCE, SCP and SCT packets for other LUNs are not allowed in between the command packets for command set sequences with 2 command packets (e.g., 06h-E0h, 00h-30h, 80h-12h, etc.).
5. For command set sequences with 12h command packet, issuance of LUNSel, SCE, SCP and SCT packets for other LUNs are allowed after the 12h command packet.
6. For command set sequences with only 1 command packet and which require address packets after the command packet, issuance of LUNSel, SCE, SCP and SCT packets for other LUNs are not allowed in between the command packet and the last address packet for the command set sequence.

Table 6-2 SCA Protocol Command Set

Reserved opcodes shall not be used by the device, as the ONFI specification may define the use of these opcodes in a future revision. Vendor specific opcodes may be used at the discretion of the vendor and shall never be defined for standard use by ONFI.

Type	Opcode
Standard Command Set	00h, 05h – 06h, 10h – 12h, 15h, 18h, 30h – 32h, 35h, 3Fh, 60h, 62h – 64h, 70h, 76h, 78h, 80h – 81h, 85h, 90h, 1Bh – 1Ch, D0h – D1h, D4h – D5h, D9h, E0h –E2h, ECh – EFh, F1h – F2h, F9h, FAh, FCh, FFh
Vendor Specific	01h – 04h, 07h – 0Ah, 0Ch – 0Fh, 13h, 16h – 17h, 19h – 1Ah, 1Dh – 2Fh, 33h – 34h, 36h – 3Eh, 40h – 5Fh, 61h, 65h – 6Fh, 71h – 75h, 77h, 79h – 7Fh, 84h, 87h – 8Dh, 8Fh, 91h – CFh, D2h – D3h, D6h – D8h, DAh – DFh, E3h – EBh, F0h, F3h – F8h, FBh, FD – Feh
Reserved	0Bh, 14h, 82h – 83h, 86h, 8Eh

Table 6-3 Opcode Reservations

6.2. Command Descriptions Format

The command descriptions in the Command Definition section are shown in Conv. Protocol format. See SCA Protocol section for equivalent diagrams.

6.3. Reset Definition

The Reset function puts the target in its default power-up state. The R/B_n value is unknown when Reset is issued; R/B_n is guaranteed to be low tWB after the Reset is issued.

Note that some feature settings are retained across Reset commands (as specified in section 8). As part of the Reset command, all LUNs are also reset. The command may be executed with the target in any state, except during power-on when Reset shall not be issued until R/B_n is set to one. The figure below defines the Reset behavior and timings:

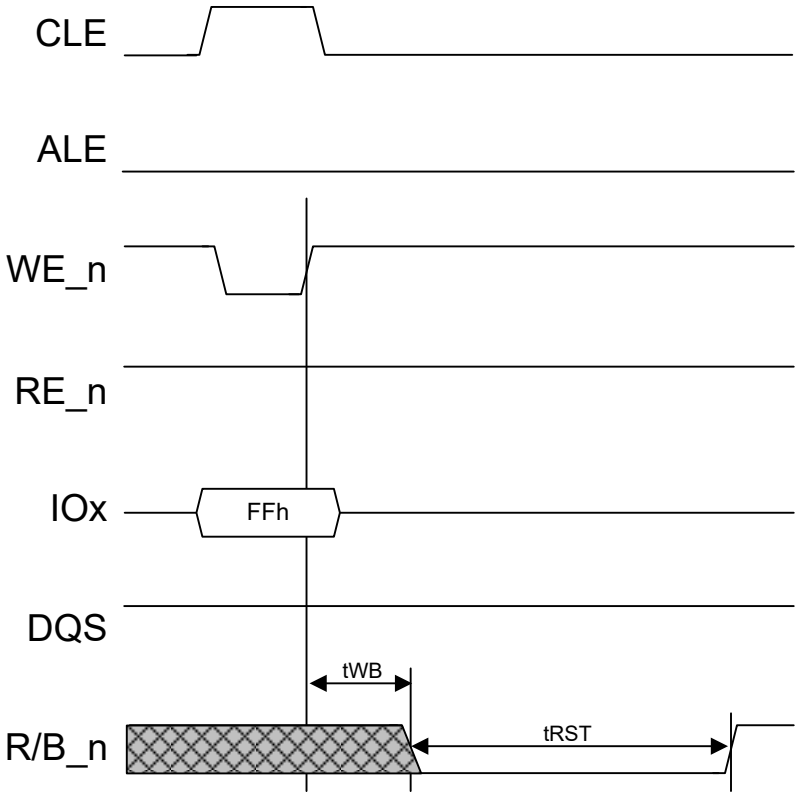


Figure 6-1 Conv. Protocol Reset Timing Diagram

6.4. Synchronous Reset Definition

The Synchronous Reset command resets the target and all LUNs. The command may be executed with the target in any state.The figure below defines the Synchronous Reset behavior and timings. The R/B_n value is unknown when Synchronous Reset is issued; R/B_n is guaranteed to be low tWB after the Synchronous Reset is issued.

This command is optional.

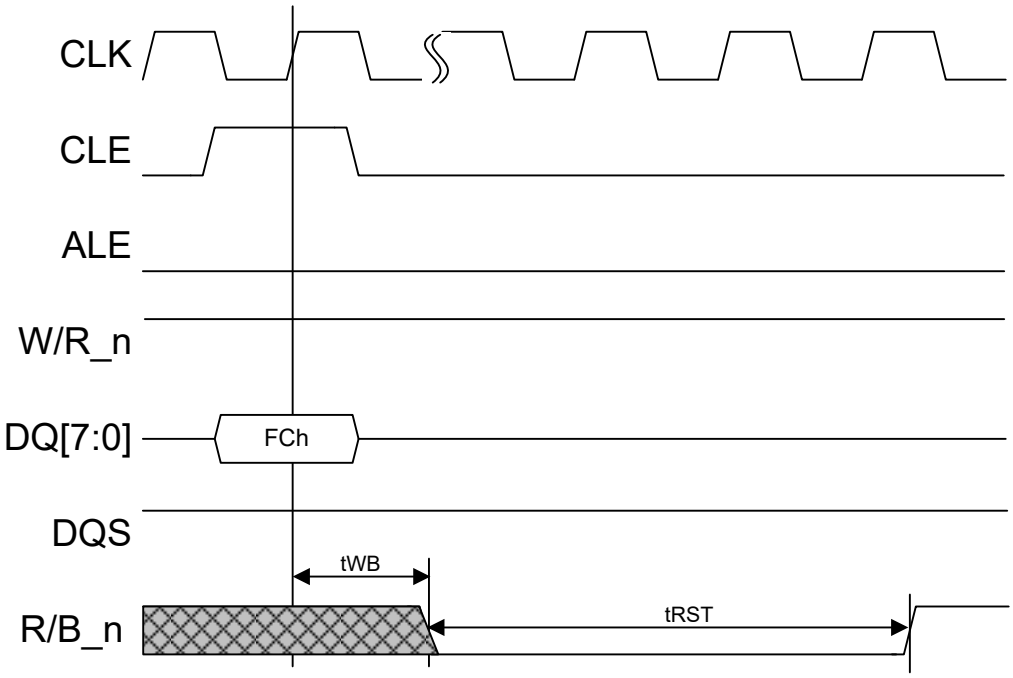


Figure 6-2 Synchronous Reset Timing Diagram

6.5. Reset LUN Definition

The Reset LUN command is used to reset a particular LUN. This command is accepted by only the LUN addressed as part of the command. The command may be executed with the LUN in any state. The figure below defines the Reset LUN behavior and timings. The SR[6] value is unknown when Reset LUN is issued; SR[6] is guaranteed to be low tWB after the Reset LUN command is issued. This command does not affect the data interface configuration for the target.

Reset LUN should be used to cancel ongoing command operations, if desired. When there are issues with the target, e.g. a hang condition, the Reset (FFh) or Synchronous Reset (FCh) commands should be used.

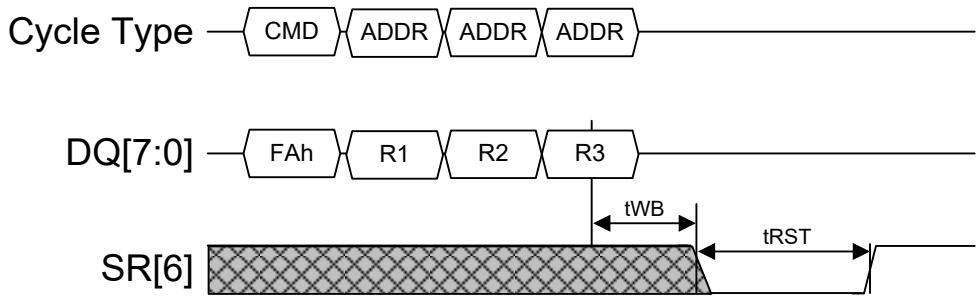


Figure 6-3 Conv. Protocol Reset LUN Timing Diagram

6.6. Read ID Definition

The Read ID function identifies device ID and whether the target supports the ONFI specification. On devices that support the ONFI specification, addresses 00h and 20h are valid.

Read ID with address 20h is used to identify if a target supports the ONFI specification. If a target supports the ONFI specification, the ONFI signature is returned. The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Read ID address 20h, Bytes 5 and 6 are Reserved and the data on those bytes are don't care.

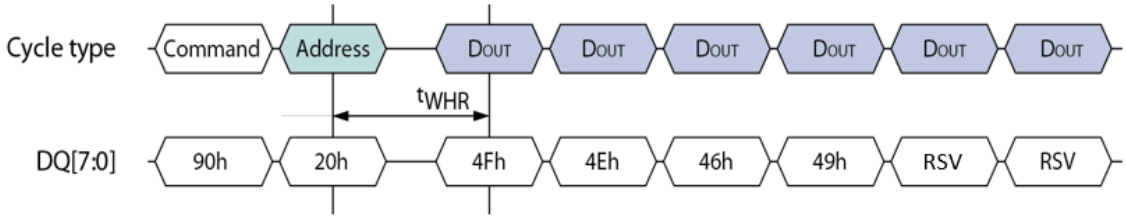


Figure 6-4 Conv. Protocol Read ID Timing Diagram for ONFI Signature

Read ID with address 00h can be used to determine the JEDEC manufacturer ID and the device ID for the particular NAND. The figure below shows the Read ID behavior and timings for retrieving the JEDEC manufacturer ID and device ID at address 00h. Reading beyond the first two bytes yields values as specified by the manufacturer.

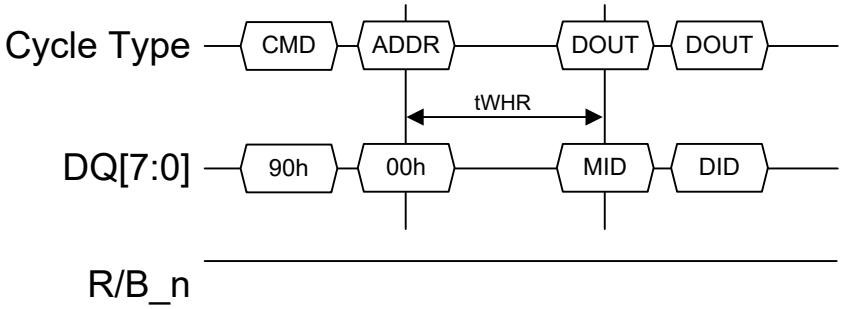


Figure 6-5 Conv. Protocol Read ID Timing Diagram for Manufacturer and Device ID

MID	Manufacturer ID for manufacturer of the part, assigned by JEDEC.
DID	Device ID for the part, assigned by the manufacturer.

Note that on the Conv. Protocol, Read ID data byte is received twice. The host shall only latch one copy of each data byte.

A more detailed timing diagram for the Conv. Protocol Read ID sequence is shown in the diagram below:

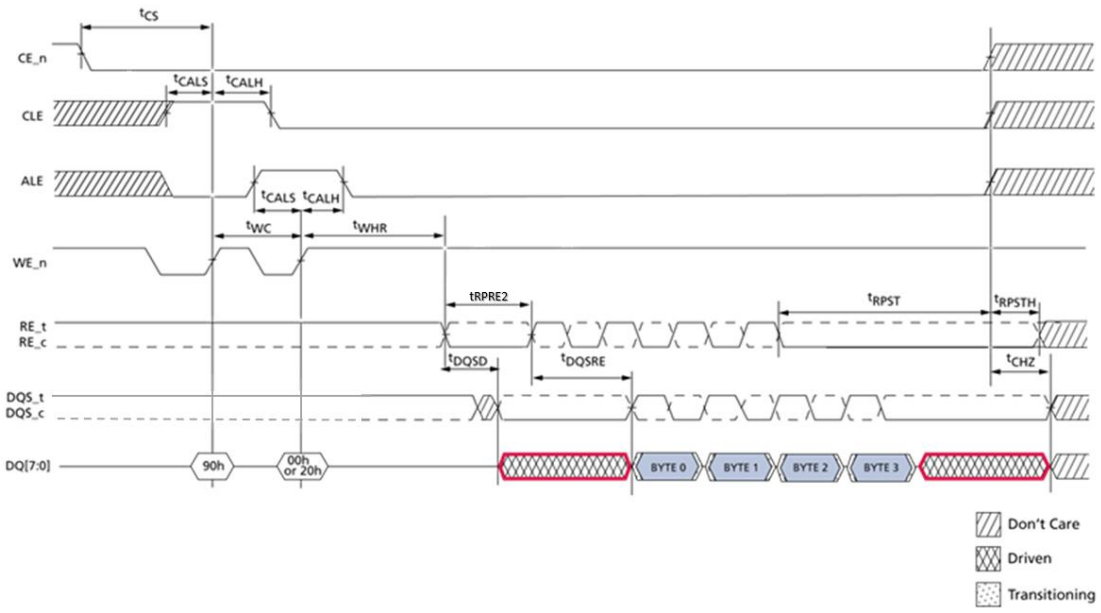


Figure 6-6 More Detailed Conv. Protocol Read ID Command Timing Diagram

NOTE 1: The data bytes in are repeated twice (on the rising and falling edge of DQS).

6.7. Read Parameter Page Definition

The Read Parameter Page function retrieves the data structure that contains information about the target. There may also be additional information provided in an extended parameter page. Values in the parameter page are static and shall not change. The host is not required to re-read the parameter page after power management related events.

The first time the host executes the Read Parameter Page command after power-on, timing mode 0 shall be used. If the host determines that the target supports more advanced timing modes, those supported timing modes may be used for subsequent execution of the Read Parameter Page command.

The Change Read Column command may be issued following execution of the Read Parameter Page to read specific portions of the parameter page.

Read Status may be used to check the status of Read Parameter Page execution.

After completion of the Read Status command, 00h may be issued by the host on the command line to output data for the Read Parameter Page command (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet).

Read Status Enhanced and Change Read Column Enhanced shall not be used during execution of the Read Parameter Page command.

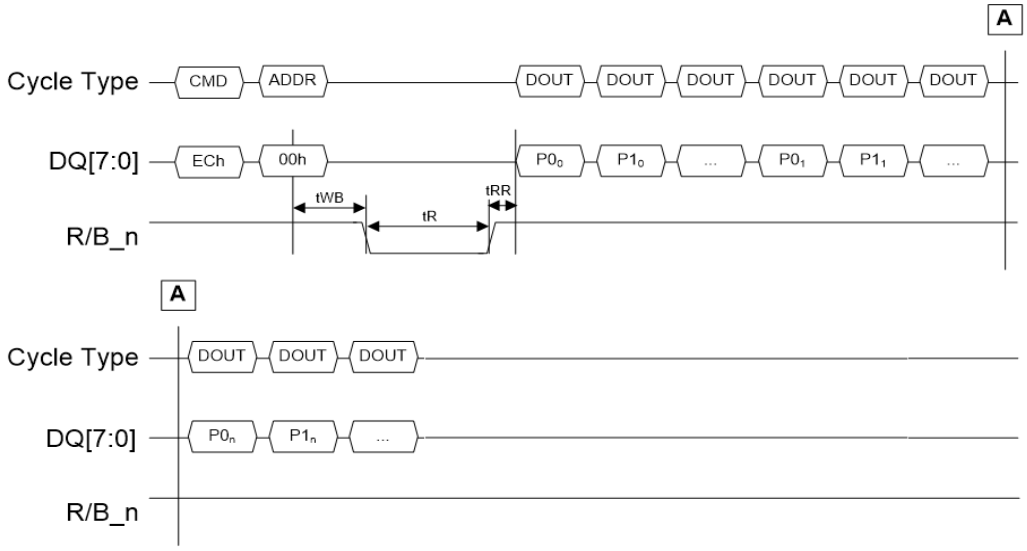


Figure 6-7 Conv. Protocol Read Parameter Page Command Timing

$P0_k$-Pn_k The kth copy of the parameter page data structure. Reading bytes beyond the end of the final parameter page copy (or beyond the final extended parameter page copy if supported) returns indeterminate values.

6.7.1. Parameter Page Data Structure Definition

The table below defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data *bytes* are in a page.

Unused fields should be cleared to 0h.

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, “O” Byte 1: 4Eh, “N” Byte 2: 46h, “F” Byte 3: 49h, “I”
4-5	M	Revision number 15 1 = supports ONFI version 6.0 14 1 = supports ONFI version 5.2 13 1 = supports ONFI version 5.1 12 1 = supports ONFI version 5.0 11 1 = supports ONFI version 4.2 10 1 = supports ONFI version 4.1 9 1 = supports ONFI version 4.0 8 1 = supports ONFI version 3.2 7 1 = supports ONFI version 3.1

Byte	O/M	Description
		6 1 = supports ONFI version 3.0 5 1 = supports ONFI version 2.3 4 1 = supports ONFI version 2.2 3 1 = supports ONFI version 2.1 2 1 = supports ONFI version 2.0 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 15 1 = supports Package Electrical Specification 14 1 = supports ZQ calibration 13 1 = supports NV-DDR3 12 1 = supports external Vpp 11 1 = supports Volume addressing 10 1 = supports NV-DDR2 9 1 = supports NV-LPDDR4 8 1 = supports program page register clear enhancement 7 1 = supports extended parameter page 6 1 = supports multi-plane read operations 5 1 = supports NV-DDR 4 1 = supports odd to even page Copyback 3 1 = supports multi-plane program and erase operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 14-15 Reserved (0) 13 1 = supports ZQ calibration (Long and Short) 12 1 = supports LUN Get and LUN Set Features 11 1 = supports ODT Configure 10 1 = supports Volume Select 9 1 = supports Reset LUN 8 1 = supports Small Data Move 7 1 = supports Change Row Address 6 1 = supports Change Read Column Enhanced 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command

Byte	O/M	Description
10	O	ONFI-JEDEC JTG primary advanced command support 4-7 Reserved (0) 3 1 = supports Multi-plane Block Erase 2 1 = supports Multi-plane Copyback Program 1 1 = supports Multi-plane Page Program 0 1 = supports Random Data Out
11	M	Training commands supported 7 1 = supports Per-Pin Vrefq Training (Absolute Value method) 6 1 = supports Per-Pin Vrefq Training (Offset method) 5 1 = supports Internal vrefq Training 4 1 = supports Write RX DQ training 3 1 = supports Write TX DQ training 2 1 = supports Read DQ training 1 1 = supports Implicit (command based) DCC training 0 1 = supports Explicit DCC Training
12-13	O	Extended parameter page length
14	O	Number of parameter pages
15	M	Training commands supported 4-7 Reserved (0) 3 1 = supports Decision Feedback Equalizer 2 1 = supports DQS Oscillator 1 1 = supports Read Duty Cycle Adjustment (RDCA) 0 1 = supports Write Duty Cycle Adjustment (WDCA)
16-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89		Reserved (0)
90-91		Reserved (0)
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	O	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	O	Bad blocks maximum per LUN
105-106	O	Block endurance
107	O	Guaranteed valid blocks at beginning of target
108-109	O	Block endurance for guaranteed valid blocks
110	O	Number of programs per page
111		Reserved (0)
112	O	Number of bits ECC correctability

Byte	O/M	Description
113	M	Number of plane address bits 4-7 Reserved (0) 0-3 Number of plane address bits
114	O	Multi-plane operation attributes 6-7 Reserved (0) 5 1 = lower bit XNOR block address restriction 4 1 = read cache supported 3 Address restrictions for cache operations 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent multi-plane support
115		Reserved (0)
116-117		Reserved (0)
118-121	O	NV-LPDDR4 timing mode support 24-31 Reserved (0) 23 1 = supports timing mode 26 22 1 = supports timing mode 25 21 1 = supports timing mode 24 20 1 = supports timing mode 23 19 1 = supports timing mode 22 18 1 = supports timing mode 21 17 1 = supports timing mode 20 16 1 = supports timing mode 19 15 1 = supports timing mode 18 14 1 = supports timing mode 17 13 1 = supports timing mode 16 12 1 = supports timing mode 15 11 1 = supports timing mode 14 10 1 = supports timing mode 13 9 1 = supports timing mode 12 8 1 = supports timing mode 11 7 1 = supports timing mode 10 6 1 = supports timing mode 9 5 1 = supports timing mode 8 4 1 = supports timing mode 7 3 1 = supports timing mode 6 2 1 = supports timing mode 5 1 1 = supports timing mode 4 0 1 = supports timing modes 0-3
122-127		Reserved (0)
	Electrical parameters block	
128		Reserved (0)
129-130		Reserved (0)
131-132		Reserved (0)
133-134		Reserved (0)
135-136		Reserved (0)
137-138		Reserved (0)
139-140		Reserved (0)
141		Reserved (0)
142		Reserved (0)

Byte	O/M	Description
143		Reserved (0)
144-145		Reserved (0)
146-147		Reserved (0)
148-149		Reserved (0)
150		Reserved (0)
151	M	Driver strength support. If the device supports NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined. 5-7 Reserved (0) 4 1 = supports 35 Ohm, 37.5 Ohm and 50 Ohm drive strength. Default is 35 Ohm 3 1 = supports 37.5 Ohm and 50 Ohm drive strength. Default is 37.5 Ohm. 2 1 = supports 18 Ohm drive strength. 1 1 = supports 25 Ohm drive strength. 0 1 = supports 35 Ohm and 50 Ohm drive strength. Default is 35 Ohm.
152-153		Reserved (0)
154-155		Reserved (0)
156-157		Reserved (0)
158		Reserved (0)
159		Reserved (0)
160-161		Reserved (0)
162		Reserved (0)
163		Reserved (0)
	Vendor block	
164-165	O	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Table 6-4 Parameter page definitions

6.7.1.1. Byte 0-3: Parameter page signature

This field contains the parameter page signature. When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Fh.

Byte 1 shall be set to 4Eh.

Byte 2 shall be set to 46h.

Byte 3 shall be set to 49h.

6.7.1.2. Byte 4-5: Revision number

This field indicates the revisions of the ONFI specification that the target complies to. The target may support multiple revisions of the ONFI specification. This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.

Bit 1 when set to one indicates that the target supports the ONFI revision 1.0 specification.

Bit 2 when set to one indicates that the target supports the ONFI revision 2.0 specification.

Bit 3 when set to one indicates that the target supports the ONFI revision 2.1 specification.

Bit 4 when set to one indicates that the target supports the ONFI revision 2.2 specification.

Bit 5 when set to one indicates that the target supports the ONFI revision 2.3 specification.

Bit 6 when set to one indicates that the target supports the ONFI revision 3.0 specification.

Bit 7 when set to one indicates that the target supports the ONFI revision 3.1 specification.

Bit 8 when set to one indicates that the target supports the ONFI revision 3.2 specification.

Bit 9 when set to one indicates that the target supports the ONFI revision 4.0 specification.

Bit 10 when set to one indicates that the target supports the ONFI revision 4.1 specification.

Bit 11 when set to one indicates that the target supports the ONFI revision 4.2 specification.

Bit 12 when set to one indicates that the target supports the ONFI revision 5.0 specification.

Bit 13 when set to one indicates that the target supports the ONFI revision 5.1 specification.
Bits 14-15 are reserved and shall be cleared to zero.

6.7.1.3. Byte 6-7: Features supported

This field indicates the optional features that the target supports.

Bit 0 when set to one indicates that the target's data bus width is 16-bits. Bit 0 when cleared to zero indicates that the target's data bus width is 8-bits. The host shall use the indicated data bus width for all ONFI commands that are defined to be transferred at the bus width (x8 or x16). Note that some commands, like Read ID, always transfer data as 8-bit only. If the NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interfaces are supported, then the data bus width shall be 8-bits.

Bit 1 when set to one indicates that the target supports multiple LUN operations (see section 3.1.3). If bit 1 is cleared to zero, then the host shall not issue commands to a LUN unless all other LUNs on the target are idle (i.e. R/B_n is set to one).

Bit 2 when set to one indicates that the target supports non-sequential page programming operations, such that the host may program pages within a block in arbitrary order. Bit 2 when cleared to zero indicates that the target does not support non-sequential page programming operations. If bit 2 is cleared to zero, the host shall program all pages within a block in order starting with page 0.

Bit 3 when set to one indicates that the target supports multi-plane program and erase operations. Refer to section 6.7.1.28.

Bit 4 when set to one indicates that there are no even / odd page restrictions for Copyback operations. Specifically, a read operation may access an odd page and then program the contents to an even page using Copyback. Alternatively, a read operation may access an even page and then program the contents to an odd page using Copyback. Bit 4 when cleared to zero indicates that the host shall ensure that Copyback reads and programs from odd page to odd page or alternatively from even page to even page.

Bit 5 when set to one indicates that the NV-DDR data interface is supported by the target. If bit 5 is set to one, then the target shall indicate the NV-DDR timing modes supported in the NV-DDR timing mode support field. Bit 5 when cleared to zero indicates that the NV-DDR data interface is not supported by the target.

Bit 6 when set to one indicates that the target supports multi-plane read operations. Refer to section 6.7.1.28.

Bit 7 when set to one indicates the target includes an extended parameter page that is stored in the data bytes following the last copy of the parameter page. If bit 7 is cleared to zero, then an extended parameter page is not supported. NOTE: This bit was inadvertently specified in the BA NAND specification to show support for BA NAND. If the device supports BA NAND, then the number of bits of ECC correctability should be cleared to 0h in byte 112 of the parameter page.

Bit 8 when set to one indicates that the target supports clearing only the page register for the LUN addressed with the Program (80h) command. If bit 8 is cleared to zero, then a Program (80h) command clears the page register for each LUN that is part of the target. At power-on, the device clears the page register for each LUN that is part of the target. Refer to section 8.1 for how to enable this feature.

Bit 9 when set to one indicates that the NV-LPDDR4 interface is supported by the target. If bit 9 is set to one, then the target shall indicate the NV-LPDDR4 timing modes supported in the NV-LPDDR4 timing mode support field. Bit 9 when cleared to zero indicates that the NV-LPDDR4 data interface is not supported by the target.

Bit 10 when set to one indicates that the NV-DDR2 data interface is supported by the target. If bit 10 is set to one, then the target shall indicate the NV-DDR2 timing modes supported in the NV-DDR2 timing mode support field. Bit 10 when cleared to zero indicates that the NV-DDR2 data interface is not supported by the target.

Bit 11 when set to one indicates that the NAND Target supports Volume addressing, as defined in section 3.2. If bit 11 is cleared to zero, then the target does not support Volume addressing.

Bit 12 when set to one indicates that the target supports external Vpp. If bit 12 is cleared to zero, then the target does not support external Vpp.

Bit 13 when set to one indicates that the NV-DDR3 data interface is supported by the target. If bit 13 is set to one, then the target shall indicate the NV-DDR3 timing modes supported in the NV-DDR3 timing mode support field. Bit 13 when cleared to zero indicates that the NV-DDR3 data interface is not supported by the target.

Bit 14 when set to one indicates that the target supports ZQ calibration. If bit 14 is cleared to zero, then the target does not support ZQ calibration.

Bit 15 when set to one indicates that the target supports Package Electrical Specification and Pad Capacitance. If bit 15 is cleared to zero, then the target does not support Package Electrical Specification and Pad Capacitance.

6.7.1.4. Byte 8-9: Optional commands supported

This field indicates the optional commands that the target supports.

Bit 0 when set to one indicates that the target supports the Page Cache Program command. If bit 0 is cleared to zero, the host shall not issue the Page Cache Program command to the target.

Bit 1 when set to one indicates that the target supports the Read Cache Random, Read Cache Sequential, and Read Cache End commands. If bit 1 is cleared to zero, the host shall not issue the Read Cache Sequential, Read Cache Random, or Read Cache End commands to the target.

Bit 2 when set to one indicates that the target supports the Get Features and Set Features commands. If bit 2 is cleared to zero, the host shall not issue the Get Features or Set Features commands to the target.

Bit 3 when set to one indicates that the target supports the Read Status Enhanced command. If bit 3 is cleared to zero, the host shall not issue the Read Status Enhanced command to the target. Read Status Enhanced shall be supported if the target has multiple LUNs or supports multi-plane operations.

Bit 4 when set to one indicates that the target supports the Copyback Program and Copyback Read commands. If bit 4 is cleared to zero, the host shall not issue the Copyback Program or Copyback Read commands to the target. If multi-plane operations are supported and this bit is set to one, then multi-plane copyback operations shall be supported.

Bit 5 when set to one indicates that the target supports the Read Unique ID command. If bit 5 is cleared to zero, the host shall not issue the Read Unique ID command to the target.

Bit 6 when set to one indicates that the target supports the Change Read Column Enhanced command. If bit 6 is cleared to zero, the host shall not issue the Change Read Column Enhanced command to the target.

Bit 7 when set to one indicates that the target supports the Change Row Address command. If bit 7 is cleared to zero, the host shall not issue the Change Row Address command to the target.

Bit 8 when set to one indicates that the target supports the Small Data Move command for both Program and Copyback operations. If bit 8 is cleared to zero, the target does not support the Small Data Move command for Program or Copyback operations. The Small Data Move command is mutually exclusive with overlapped multi-plane support. Refer to section 6.19. When bit 8 is set to one, the device shall support the 11h command to flush any internal data pipeline regardless of whether multi-plane operations are supported.

Bit 9 when set to one indicates that the target supports the Reset LUN command. If bit 9 is cleared to zero, the host shall not issue the Reset LUN command.

Bit 10 when set to one indicates that the target supports the Volume Select command. If bit 10 is cleared to zero, the host shall not issue the Volume Select command. The device shall support the Volume Select command if it supports either the CE_n pin reduction or matrix termination features.

Bit 11 when set to one indicates that the target supports the ODT Configure command. If bit 11 is cleared to zero, the host shall not issue the ODT Configure command. The device shall support the ODT Configure command if it supports the matrix termination feature.

Bit 12 when set to one indicates that the target supports the LUN Get Features and LUN Set Features commands. If bit 12 is cleared to zero, the host shall not issue the LUN Get Features or LUN Set Features commands to the target.

Bit 13 when set to one indicates that the target supports the ZQ Calibration Long and ZQ Calibration Short commands. If bit 13 is cleared to zero, the host shall not issue ZQ Calibration Long or ZQ Calibration Short commands.

Bits 14-15 are reserved and shall be cleared to zero.

6.7.1.5. Byte 10: ONFI-JEDEC JTG primary advanced command support

This field indicates the primary advanced commands defined by the ONFI-JEDEC Joint Taskgroup that are supported by the target. Specifically, these are commands where the primary version of the advanced commands is not based on an ONFI heritage. Support for primary advanced commands that are based on an ONFI heritage are indicated in their traditional parameter page location.

Bit 0 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Random Data Out command. If bit 0 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Random Data Out command to the target. Specifically, the ONFI-JEDEC JTG primary Random Data Out command is the sequence 00h - Column and Row Address Cycles Input - 05h - Column Address Cycles Input - E0h. Refer to the vendor device datasheet for the number of address cycles needed after the 00h and 05h commands.

Bit 1 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Multi-plane Page Program command. If bit 1 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Multi-plane Page Program command to the target. Specifically, the ONFI-JEDEC JTG primary Multi-plane Page Program command utilizes 81h for the first cycle of program sequences after the initial program sequence instead of 80h.

Bit 2 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Multi-plane Copyback Program command. If bit 2 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Multi-plane Copyback Program command to the target. Specifically, the ONFI-JEDEC JTG primary Multi-plane Copyback Program command utilizes 81h for the first cycle of program sequences after the initial program sequence instead of 85h.

Bit 3 when set to one indicates that the target supports the ONFI-JEDEC JTG primary Multi-plane Block Erase command. If bit 3 is cleared to zero, the host shall not issue the ONFI-JEDEC JTG primary Multi-plane Block Erase command to the target. Specifically, the ONFI-JEDEC JTG primary Multi-plane Block Erase does not utilize the D1h command cycle between block addresses.

Bits 4-7 are reserved and shall be cleared to zero.

6.7.1.6. Byte 11: Training Commands Support

This field indicates the training commands supported as defined by the ONFI-JEDEC Joint Taskgroup that are supported by the target.

Bit 0 when set to one indicates that the target supports Explicit DCC training. If bit 0 is cleared to zero, the host does not support Explicit DCC training. Specifically, Explicit DCC training is initiated with a Set Features command (EFh) at B0[0] of feature address 20h.

Bit 1 when set to one indicates that the target supports Implicit (command based) DCC training. If bit 1 is cleared to zero, the host does not support Implicit (command based) DCC training. Specifically, Implicit DCC training is initiated with an Implicit DCC training command (18h) along with a targeted address.

Bit 2 when set to one indicates that the target supports Read DQ training. If bit 2 is cleared to zero, the host does not support Read DQ training. Specifically, Read DQ training is initiated with a Read DQ training command (62h) along with a targeted address.

Bit 3 when set to one indicates that the target supports Write DQ TX training. If bit 3 is cleared to zero, the host does not support Write DQ TX training. Specifically, Write DQ TX training is initiated with command 63h along with a targeted address and read back using command 64h.

Bit 4 when set to one indicates that the target supports Write DQ RX training. If bit 4 is cleared to zero, the host does not support Write DQ RX training. Specifically, Write DQ RX training is initiated with command 76h along with a targeted address.

Bit 5 when set to one indicates that the target supports Internal Vrefq Training. If bit 5 is cleared to zero, the host does not support Internal Vrefq Training.

Bit 6 when set to one indicates that the target supports Per-Pin Vrefq Training by Offset method. If bit 6 is cleared to zero, the host does not support Per-Pin Vrefq Training by Offset method.

Bit 7 when set to one indicates that the target supports Per-Pin Vrefq Training by Absolute Value method. If bit 7 is cleared to zero, the host does not support Per-Pin Vrefq Training by Absolute Value method.

6.7.1.7. Byte 12-13: Extended parameter page length

If the target supports an extended parameter page as indicated in the Features supported field, then this field specifies the length of the extended parameter page in multiples of 16 bytes. Thus, a value of 2 corresponds to 32 bytes and a value of 3 corresponds to 48 bytes. The minimum size is 3, corresponding to 48 bytes.

6.7.1.8. Byte 14: Number of parameter pages

If the target supports an extended parameter page as indicated in the Features supported field, then this field specifies the number of parameter pages present, including the original and the subsequent redundant versions. As an example, a value of 3 means that there are three parameter pages present and thus the extended parameter page starts at byte 768. The number of extended parameter pages should match the number of parameter pages.

6.7.1.9. Byte 15: Additional Training Commands Support

This field indicates the additional training commands supported as defined by the ONFI-JEDEC Joint Taskgroup that are supported by the target.

Bit 0 when set to one indicates that the target supports Write Duty Cycle Training. If bit 0 is cleared to zero, the host does not support Write Duty-Cycle Adjustment

Bits 1-7 are reserved and shall be cleared to zero.

6.7.1.10. Byte 32-43: Device manufacturer

This field contains the manufacturer of the device. The content of this field is an ASCII character string of twelve bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string. If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID (refer to section 6.7.1.12).

6.7.1.11. Byte 44-63: Device model

This field contains the model number of the device. The content of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

6.7.1.12. Byte 64: JEDEC manufacturer ID

This field contains the JEDEC manufacturer ID for the manufacturer of the device.

6.7.1.13. Byte 65-66: Date code

This field contains a date code for the time of manufacture of the device. Byte 65 shall contain the two least significant digits of the year (e.g. a value of 05h to represent the year 2005). Byte 66 shall contain the workweek, where a value of 00h indicates the first week of January.

If the date code functionality is not implemented, the value in this field shall be 0000h.

6.7.1.14. Byte 80-83: Number of data bytes per page

This field contains the number of data bytes per page. The value reported in this field shall be a power of two. The minimum value that shall be reported is 512 bytes.

6.7.1.15. Byte 84-85: Number of spare bytes per page

This field contains the number of spare bytes per page. There are no restrictions on the value.

6.7.1.16. Byte 92-95: Number of pages per block

This field contains the number of pages per block. This value shall be a multiple of 32. Refer to section 3.1 for addressing requirements.

6.7.1.17. Byte 96-99: Number of blocks per logical unit

This field contains the number of blocks per logical unit. There are no restrictions on this value. Refer to section 3.1 for addressing requirements.

6.7.1.18. Byte 100: Number of logical units (LUNs)

This field indicates the number of logical units the target supports. Logical unit numbers are sequential, beginning with a LUN address of 0. This field shall be greater than zero.

6.7.1.19. Byte 101: Number of Address Cycles

This field indicates the number of address cycles used for row and column addresses. The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.

Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE: Throughout this specification examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

6.7.1.20. Byte 102: Number of bits per cell

This field indicates the number of bits per cell in the Flash array. This field shall be greater than zero.

A value of FFh indicates that the number of bits per cell is not specified.

6.7.1.21. Byte 103-104: Bad blocks maximum per LUN

This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN. The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in the parameter page.

6.7.1.22. Byte 105-106: Block endurance

This field indicates the maximum number of program/erase cycles per addressable page/block. This value assumes that the host is using at least the minimum ECC correctability reported in the parameter page.

A page may be programmed in partial operations subject to the value reported in the Number of programs per page field. However, programming different locations within the same page does not count against this value more than once per full page.

The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 105 comprises the value. Byte 106 comprises the multiplier. For example, a target with an endurance of 75,000 cycles would report this as a value of 75 and a multiplier of 3 (75 x 10^3). For a write once device, the target shall report a value of 1 and a multiplier of 0. For a read-only device, the target shall report a value of 0 and a multiplier of 0. The value field shall be the smallest possible; for example, 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 10^5).

6.7.1.23. Byte 107: Guaranteed valid blocks at beginning of target

This field indicates the number of guaranteed valid blocks starting at block address 0 of the target. The minimum value for this field is 1h. The blocks are guaranteed to be valid for the endurance specified for this area (see section 6.7.1.24) when the host follows the specified number of bits to correct.

6.7.1.24. Byte 108-109: Block endurance for guaranteed valid blocks

This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area (see section 6.7.1.23). This value requires that the host is using at least the minimum ECC correctability reported in the parameter page. This value is not encoded. If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

6.7.1.25. Byte 110: Number of programs per page

This field indicates the maximum number of times a portion of a page may be programmed without an erase operation. After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page. This field shall be greater than zero. Programming the same portion of a page without an erase operation results in indeterminate page contents.

6.7.1.26. Byte 112: Number of bits ECC correctability

This field indicates the number of bits that the host should be able to correct per 512 bytes of data. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in the parameter page. When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks shall not be exceeded by the device. All used bytes in the page shall be protected by host controller ECC including the spare bytes if the minimum ECC requirement has a value greater than zero.

If the recommended ECC codeword size is not 512 bytes, then this field shall be set to FFh. The host should then read the Extended ECC Information that is part of the extended parameter page to retrieve the ECC requirements for this device.

When this value is cleared to zero, the target shall return valid data.

6.7.1.27. Byte 113: Multi-plane addressing

This field describes parameters for multi-plane addressing.

Bits 0-3 indicate the number of bits that are used for multi-plane addressing. This value shall be greater than 0h when multi-plane operations are supported. For information on the plane address location, refer to section 3.1.1.

Bits 4-7 are reserved.

6.7.1.28. Byte 114: Multi-plane operation attributes

This field describes attributes for multi-plane operations. This byte is mandatory when multi-plane operations are supported as indicated in the Features supported field.

Bit 0 indicates whether overlapped multi-plane operations are supported. If bit 0 is set to one, then overlapped multi-plane operations are supported. If bit 0 is cleared to zero, then concurrent multi-plane operations are supported.

Bit 1 indicates that there are no block address restrictions for the multi-plane operation. If set to one all block address bits may be different between multi-plane operations. If cleared to zero, there are block address restrictions. Refer to bit 5 for the specific block address restrictions required.

Bit 2 indicates whether program cache is supported with multi-plane programs. If set to one then program cache is supported for multi-plane program operations. If cleared to zero then program cache is not supported for multi-plane program operations. Note that program cache shall not be used with multi-plane copyback program operations. See bit 3 for restrictions on the multi-plane addresses that may be used.

Bit 3 indicates whether the block address bits other than the multi-plane address bits of multi-plane addresses may change during either: a) a program cache sequence between 15h commands, or b) a read cache sequence between 31h commands. If set to one and bit 2 is set to

one, then the host may change the number of multi-plane addresses and the value of the block address bits (other than the multi-plane address bits) in the program cache sequence. If set to one and bit 4 is set to one, then the host may change the number of multi-plane addresses and the value of the block address bits (other than the multi-plane address bits) in the read cache sequence. If cleared to zero and bit 2 is set to one, then for each program cache operation the block address bits (other than the plane address bits) and number of multi-plane addresses issued to the LUN shall be the same. If cleared to zero and bit 4 is set to one, then for each read cache operation the block address bits (other than the multi-plane address bits) and number of multi-plane addresses issued to the LUN shall be the same.

Bit 4 indicates whether read cache is supported with multi-plane reads. If set to one then read cache is supported for multi-plane read operations. If cleared to zero then read cache is not supported for multi-plane read operations. Note that read cache shall not be used with multi-plane copyback read operations.

Bit 5 indicates the type of block address restrictions required for the multi-plane operation. If set to one then all block address bits (other than the multi-plane address bits) shall be the same if the XNOR of the lower multi-plane address bits between two multi-plane addresses is one. If cleared to zero, all block address bits (other than the multi-plane address bits) shall be the same regardless of the multi-plane address bits between two plane addresses. See section 3.1.1.1 for a detailed definition of interleaved block address restrictions. These restrictions apply to all multi-plane operations (Read, Program, Erase, and Copyback Program).

Bits 6-7 are reserved.

6.7.1.29. Byte 116-117: NV-DDR3 timing mode support (cont.)

This field indicates the NV-DDR3 timing modes above mode 18 that are supported. If the NV-DDR3 data interface is supported by the target, at least one NV-DDR3 timing mode shall be supported. The target shall support an inclusive range of NV-DDR3 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR3 timing modes 19.

Bit 1 when set to one indicates that the target supports NV-DDR3 timing modes 20.

Bit 2 when set to one indicates that the target supports NV-DDR3 timing modes 21.

Bit 3 when set to one indicates that the target supports NV-DDR3 timing modes 22.

Bits 4-15 are reserved.

6.7.1.30. Byte 118-121: NV-LPDDR4 timing mode support

This field indicates the NV-LPDDR4 timing modes supported. If the NV-LPDDR4 data interface is supported by the target, at least one NV-LPDDR4 timing mode shall be supported. The target shall support an inclusive range of NV-LPDDR4 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-LPDDR4 timing modes 0-3.

Bit 1 when set to one indicates that the target supports NV-LPDDR4 timing mode 4.

Bit 2 when set to one indicates that the target supports NV-LPDDR4 timing mode 5.

Bit 3 when set to one indicates that the target supports NV-LPDDR4 timing mode 6.

Bit 4 when set to one indicates that the target supports NV-LPDDR4 timing mode 7.

Bit 5 when set to one indicates that the target supports NV-LPDDR4 timing mode 8.

Bit 6 when set to one indicates that the target supports NV-LPDDR4 timing mode 9.

Bit 7 when set to one indicates that the target supports NV-LPDDR4 timing mode 10.

Bit 8 when set to one indicates that the target supports NV-LPDDR4 timing mode 11.

Bit 9 when set to one indicates that the target supports NV-LPDDR4 timing mode 12.

Bit 10 when set to one indicates that the target supports NV-LPDDR4 timing mode 13.

Bit 11 when set to one indicates that the target supports NV-LPDDR4 timing mode 14.

Bit 12 when set to one indicates that the target supports NV-LPDDR4 timing mode 15.

Bit 13 when set to one indicates that the target supports NV-LPDDR4 timing mode 16.

Bit 14 when set to one indicates that the target supports NV-LPDDR4 timing mode 17.

Bit 15 when set to one indicates that the target supports NV-LPDDR4 timing mode 18.

Bit 16 when set to one indicates that the target supports NV-LPDDR4 timing mode 19.

Bit 17 when set to one indicates that the target supports NV-LPDDR4 timing mode 20.

Bit 18 when set to one indicates that the target supports NV-LPDDR4 timing mode 21.

Bit 19 when set to one indicates that the target supports NV-LPDDR4 timing mode 22.

6.7.1.31. Byte 129-130: Reserved

6.7.1.32. Byte 141: Reserved

6.7.1.33. Byte 142: Reserved

6.7.1.34. Byte 143: NV-DDR / NV-DDR2 / NV-DDR3 / NV-LPDDR4 features

This field describes features and attributes for NV-DDR, NV-DDR2, NV-DDR3 and/or NV-LPDDR4 operation. This byte is mandatory when the NV-DDR or NV-DDR2 data interface is supported.

Bit 0 indicates the tCAD value that shall be used by the host. If bit 0 is set to one, then the host shall use the tCADs (slow) value in NV-DDR command, address and data transfers. If bit 0 is cleared to zero, then the host shall use the tCADf (fast) value in NV-DDR command, address and data transfers. This field applies to the NV-DDR data interface only.

Bit 1 is reserved

Bit 2 indicates that the device supports the CLK being stopped during data input, as described in **Error! Reference source not found.**. If bit 2 is set to one, then the host may optionally stop the CLK during data input for power savings. If bit 2 is set to one, the host may pause data while the

CLK is stopped. If bit 2 is cleared to zero, then the host shall leave CLK running during data input. This field applies to the NV-DDR data interface only.

Bit 3 indicates that the device requires the power-on sequence to provide valid Vcc before Vpp and the power-down sequence to remove Vpp before removing Vcc.

Bits 4-7 are reserved.

6.7.1.35. Byte 151: Driver strength support

This field describes if the target supports configurable driver strengths and its associated features. If the device supports NV-DDR, NV-DDR2, NV-DDR3 or NV-LPDDR4 data interface, then one and only one of bit 0, bit 3, and bit 4 shall be set. If bit 0, bit 3, and bit 4 are all cleared to zero, then the driver strength at power-on is undefined.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in **Error! Reference source not found.**. If this bit is set to one, then the device shall support both the 35 Ohm and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 35 Ohm value defined in **Error! Reference source not found.**.

Bit 1 when set to one indicates that the target supports the 25 Ohm setting in for use in the I/O Drive Strength setting.

Bit 2 when set to one indicates that the target supports the 18 Ohm setting for use in the I/O Drive Strength setting.

Bit 3 when set to one indicates that the target supports configurable driver strength settings. If this bit is set to one, then the device shall support both the 37.5 Ohm and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 37.5 Ohm value.

Bit 4 when set to one indicates that the target supports configurable driver strength settings. If this bit is set to one, then the device shall support the 35 Ohm, 37.5 Ohm, and 50 Ohm settings. If this bit is set to one, then the device shall power-on with a driver strength at the 35 Ohm value.

Bits 5-7 are reserved.

6.7.1.36. Byte 158: NV-DDR2/3 and NV-LPDDR4 features

This field describes features and attributes for NV-DDR2 and NV-DDR3 operation. This byte is mandatory when the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface is supported.

Bit 0 indicates if self-termination ODT is supported. If bit 0 is set to one, then self-termination ODT is supported. If bit 0 is cleared to zero, then self-termination ODT is not supported and the host shall not enable ODT. Refer to section 4.13.

Bit 1 indicates if matrix termination ODT is supported. If bit 1 is set to one, then matrix termination ODT is supported. If bit 1 is cleared to zero, then matrix termination ODT is not supported and the host shall not issue the ODT Configure command. If matrix termination ODT is supported, then the device shall also support self-termination ODT. Refer to section 4.13.

Bit 2 indicates if the optional on-die termination value of 30 Ohms is supported. If bit 2 is set to one, then the on-die termination value of 30 Ohms is supported. If bit 2 is cleared to zero, then the on-die termination value of 30 Ohms is not supported and the host shall not select that value.

Bit 3 indicates if the optional differential signaling for RE_n is supported. If bit 3 is set to one, then differential signaling for RE_n is supported. If bit 3 is cleared to zero, then differential signaling for RE_n is not supported. Refer to section 4.10.1.

Bit 4 indicates if the optional differential signaling for DQS is supported. If bit 4 is set to one, then differential signaling for DQS is supported. If bit 4 is cleared to zero, then differential signaling for DQS is not supported. Refer to section 4.10.1.

Bit 5 indicates if external VREFQ is required for speeds ≥ 200 MT/s. If bit 5 is set to one, then external VREFQ is required and VEN shall be set to one by the host when using timing modes with speeds ≥ 200 MT/s (refer to section 8.2). If bit 5 is cleared to zero, then external VREFQ is optional for use by the host when using timing modes with speeds ≥ 200 MT/s.

Bits 6-7 are reserved.

6.7.1.37. Byte 159: NV-DDR2/3 and NV-LPDDR4 warmup cycles

This field describes support for warmup cycles for NV-DDR2 NV-DDR3 or NV-LPDDR4 operation. Warmup cycles are defined in section 4.12. This byte is mandatory when the NV-DDR2 NV-DDR3 or NV-LPDDR4 data interface is supported.

Bits 0-3 indicate the number of warmup cycles that are supported for data output operation. If this field is cleared to 0h, then the target does not support warmup cycles for data output operation. The host shall not configure the target to a number of warmup cycles that exceeds the value provided. Refer to section 8.2 for details on configuring the number of warmup cycles for data output.

Bits 4-7 indicate the number of warmup cycles that are supported for data input operation. If this field is cleared to 0h, then the target does not support warmup cycles for data input operation. The host shall not configure the target to a number of warmup cycles that exceeds the value provided. Refer to section 8.2 for details on configuring the number of warmup cycles for data input.

6.7.1.38. Byte 160-161: Reserved

6.7.1.39. Byte 162: NV-DDR2 timing mode support

This field is a continuation of Byte 142. This field indicates the NV-DDR2 timing modes supported. If the NV-DDR2 data interface is supported by the target, at least one NV-DDR2 timing mode shall be supported. The target shall support an inclusive range of NV-DDR2 timing modes (i.e. if timing mode n-1 and n+1 are supported, then the target shall also support timing mode n).

Bit 0 when set to one indicates that the target supports NV-DDR2 timing mode 8.

Bit 1 when set to one indicates that the target supports NV-DDR3 timing mode 9.

Bit 2 when set to one indicates that the target supports NV-DDR3 timing mode 10.

Bits 3-7 are reserved and shall be cleared to zero.

6.7.1.40. Byte 164-165: Vendor specific Revision number

This field indicates a vendor specific revision number. This field should be used by vendors to indicate the supported layout for the vendor specific parameter page area and the vendor specific feature addresses. The format of this field is vendor specific.

6.7.1.41. Byte 166-253: Vendor specific

This field is reserved for vendor specific use.

6.7.1.42. Byte 254-255: Integrity CRC

The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 253 of the parameter page inclusive.

The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:

$G(X) = X_{16} + X_{15} + X_2 + 1$

This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

6.7.1.43. Byte 256-511: Redundant Parameter Page 1

This field shall contain the values of bytes 0-255 of the parameter page. Byte 256 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-255. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 256 bytes.

6.7.1.44. Byte 512-767: Redundant Parameter Page 2

This field shall contain the values of bytes 0-255 of the parameter page. Byte 512 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-255 and in the first redundant parameter page. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 256 bytes.

6.7.1.45. Byte 768+: Additional Redundant Parameter Pages

Bytes at offset 768 and above may contain additional redundant copies of the parameter page. There is no limit to the number of redundant parameter pages that the target may provide. The target may provide additional copies to guard against the case where all three mandatory copies have invalid CRC checks.

The host should determine whether an additional parameter page is present by checking the first Dword. If at least two out of four bytes match the parameter page signature, then an additional parameter page is present.

6.8. Read Unique ID Definition

The Read Unique ID function is used to retrieve the 16-byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement, as shown in the table below. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid.

Bytes	Value
0-15	UID
16-31	UID complement (bitwise)

Table 6-5 UID and Complement

To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

Read Status Enhanced shall not be used during execution of the Read Unique ID command.

The figure below defines the Read Unique ID sequence on the Conv. Protocol. The host may use any timing mode supported by the target in order to retrieve the UID data.

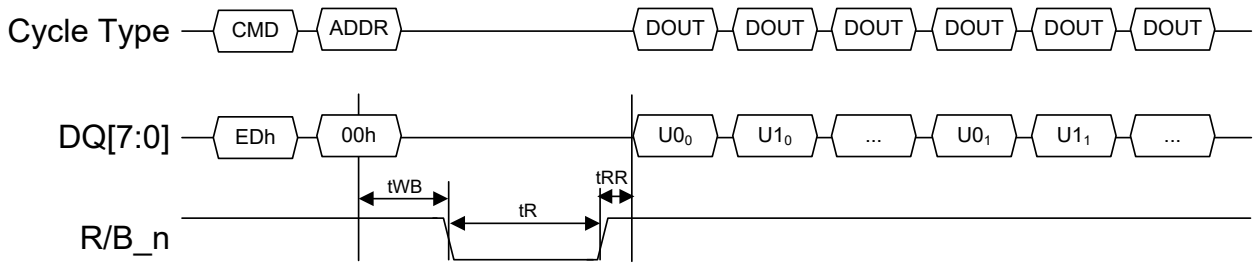


Figure 6-8 Conv. Protocol Read Unique ID Timing

$U0_k$-Un_k The kth copy of the UID and its complement. Sixteen copies are stored. Reading beyond 512 bytes returns indeterminate values.

6.9. Block Erase Definition

The Block Erase function erases the block of data identified by the block address parameter on the LUN specified. A Block Erase operation shall be considered successful if SR[0] returns a zero after completion of the Block Erase operation. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. The figure below defines the Block Erase behavior and timings on the Conv. Protocol.

If the host attempts to erase a factory marked bad block, then the device shall not proceed with the requested operation and shall set the FAIL bit to one for the operation.

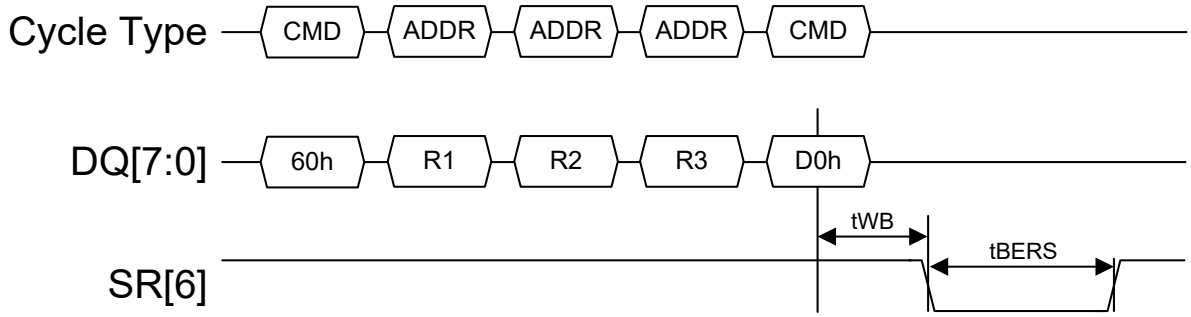


Figure 6-9 Conv. Protocol Block Erase Timing

R1-R3 The row address of the block to be erased. R1 is the least significant byte in the row address.

6.10. Read Status Definition

In the case of non-multi-plane operations, the Read Status function retrieves a status value for the last operation issued. If multiple multi-plane operations are in progress on a single LUN, then Read Status returns the composite status value for status register bits that are independent per plane address. Specifically, Read Status shall return the combined status value of the independent status register bits according to the table below (see Status Field Definition section for status register bit definitions):

Status Register bit	Composite status value
Bit 0, FAIL	OR
Bit 1, FAILC	OR

Table 6-6 Composite Status Value

The figure below defines the Conv. Protocol Read Status behavior and timings. Note that each data output byte is received twice. The host shall only latch one copy of each data byte.

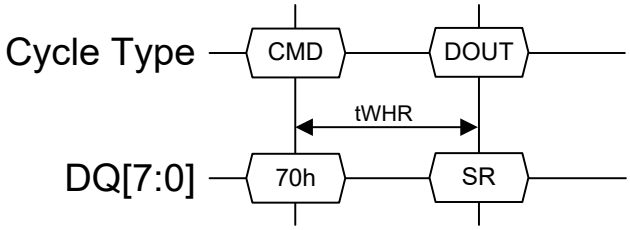


Figure 6-10 Conv. Protocol Read Status Timing

SR Status value as defined in Status Field Definition section

A more detailed timing diagram for the Conv. Protocol Read Status sequence, applicable to both NV-LPDDR4 and NV-LPDDR4 with VccQL interfaces is provided in the figure below:

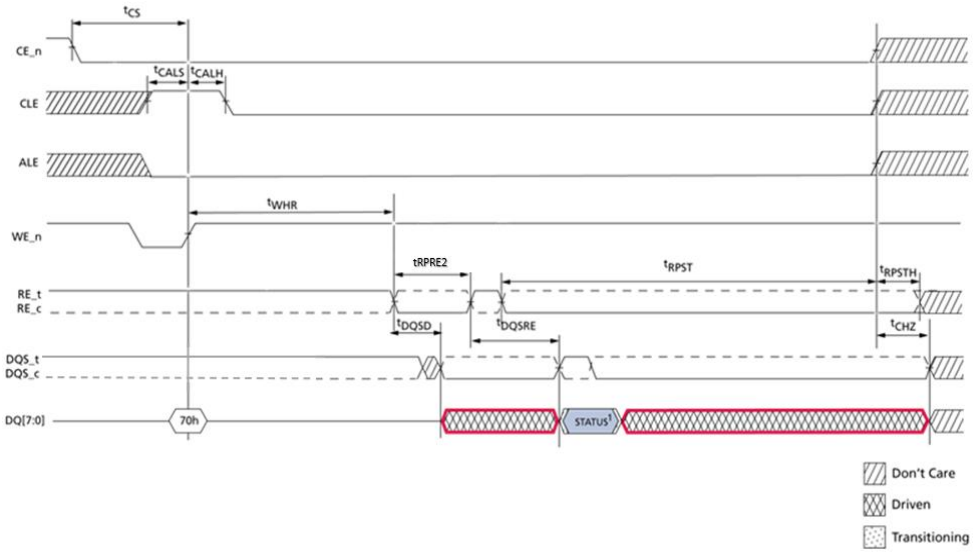


Figure 6-11 More Detailed Conv. Protocol Read Status Timing Diagram

NOTE 1: It is optional for the device to update status while RE_n is held low. If the device supports updating status while RE_n is held low, then the host may continually read updated status as the DQ[7:0] data values are updated. However, DQS only transitions based on RE_n

transitions. If the device does not support updating status while RE_n is held low, then the status will be updated based on RE_n transitions.

6.11. Read Status Enhanced Definition

The Read Status Enhanced function retrieves the status value for a previous operation on a particular LUN and plane address. The figure below defines the Read Status Enhanced behavior and timings.

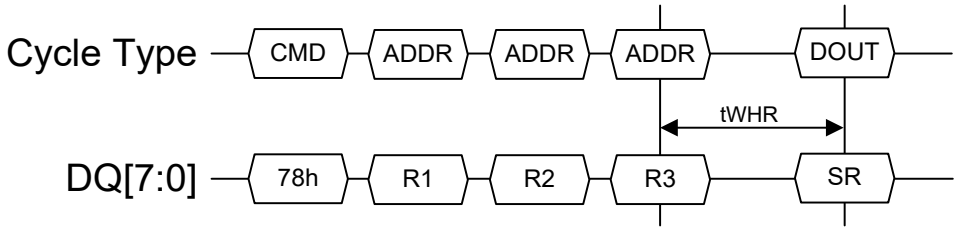


Figure 6-12 Conv. Protocol Read Status Enhanced Timing

R1-R3 Row address that contains the LUN and plane address to retrieve status for. Row address bits not associated with the LUN and plane address are not used. R1 is the least significant byte.

SR Status value as defined in Status Field Definition section.

If the row address entered is invalid, the Status value returned has an indeterminate value. The host uses Read Status Enhanced for LUN selection (refer to section 3.1.2). Note that Read Status Enhanced has no effect on which page register is selected for data output within the LUN.

When issuing Read Status Enhanced in the Conv. Protocol, each data byte is received twice. The host shall only latch one copy of each data byte.

6.12. Read Status and Read Status Enhanced Usage (Conv. Protocol Only)

In certain sequences only one status command shall be used by the host. This section outlines situations in which a particular status command is required to be used.

If a command is issued to a LUN while R/B_n is cleared to zero, then the next status command shall be Read Status Enhanced. Read Status Enhanced causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Read Status Enhanced commands responds to a subsequent toggle of the RE_n input signal.

When the host has issued Read Page commands to multiple LUNs at the same time, the host shall issue Read Status Enhanced before reading data from either LUN. Read Status Enhanced causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Read Status Enhanced commands responds to a subsequent toggle of the RE_n input signal after data output is selected with the 00h command (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet) . Refer to section 3.1.3 for additional requirements if a Change Read Column (Enhanced) command is used as part of a multiple LUN read sequence.

During and after Target level commands, the host shall not issue the Read Status Enhanced command. In these sequences, the host uses Read Status to check for the status value. The only exception to this requirement is if commands were outstanding to multiple LUNs when a Reset was issued. In this case, the Read Status Enhanced command shall be used to determine when each active LUN has completed Reset.

6.13. Status Field Definition

The returned status register byte value (SR) for Read Status and Read Status Enhanced has the format described below. If the RDY bit is cleared to zero, all other bits in the status byte (except WP_n) are invalid and shall be ignored by the host.

Value	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Status Register	WP_n	RDY	ARDY	VSP	VSP	VSP	FAILC	FAIL

FAIL If set to one, then the last command failed. If cleared to zero, then the last command was successful. This bit is only valid for program and erase operations. During program cache operations, this bit is only valid when ARDY is set to one. In devices that support ZQ calibration, this bit is set to one if the ZQ calibration operation failed.

FAILC If set to one, then the command issued prior to the last command failed. If cleared to zero, then the command issued prior to the last command was successful. This bit is only valid for program cache operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Page Cache Program sequence. When program cache is not supported, this bit is not used and shall be cleared to zero.

ARDY If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (RDY is cleared to zero) or an array operation in progress. When overlapped multi-plane operations or cache commands are not supported, this bit is not used.

RDY If set to one, then the LUN or plane address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and SR bits [5:0] are invalid and shall be ignored by the host. This bit impacts the value of R/B_n, refer to section 2.13.2. When caching operations are in use, then this bit indicates whether another command can be accepted, and ARDY indicates whether the last operation is complete.

WP_n If set to one, then the device is not write-protected. If cleared to zero, then the device is write-protected. This bit shall always be valid regardless of the state of the RDY bit.

R Reserved (0)

VSP Vendor Specific

6.14. Read Definition

The Read function reads a page of data identified by a row address for the LUN specified. The page of data is made available to be read from the page register starting at the column address specified.

The figure below defines the Conv. Protocol Read behavior and timings.

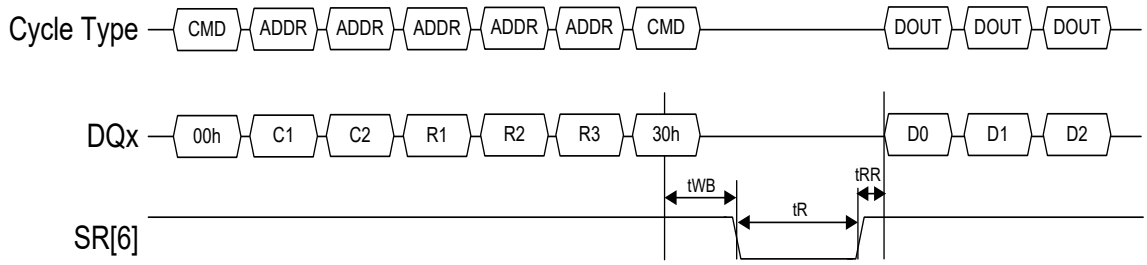


Figure 6-13 Conv. Protocol Read Timing

C1-C2 Column address of the page to retrieve. C1 is the least significant byte.

R1-R3 Row address of the page to retrieve. R1 is the least significant byte.

Dn Data bytes read from the addressed page.

Reading beyond the end of a page results in indeterminate values being returned to the host.

While monitoring the status register to determine when the tR (transfer from Flash array to page register) is complete, the host may re-issue a command value of 00h to start reading data (NOTE: Some NAND vendors may require the use of Change Read Column sequence instead of 00h command to output data from the NAND, see vendor datasheet). Issuing a command value of 00h will cause data to be returned starting at the selected column address.

6.15. Read Cache Definition

The Read Cache Sequential and Read Cache Random functions permit a page to be read from the page register while another page is simultaneously read from the Flash array for the selected LUN. A Read Page command, as defined in section 6.14, shall be issued prior to the initial Read Cache Sequential or Read Cache Random command in a read cache sequence. A Read Cache Sequential or Read Cache Random command shall be issued prior to a Read Cache End (3Fh) command being issued.

The Read Cache (Sequential or Random) function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache (Sequential or Random) function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache (Sequential or Random) function. Issuing an additional Read Cache (Sequential or Random) function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a Read Cache Sequential (31h) command after the last page of a block is read. If commands are issued to multiple LUNs at the same time, the host shall execute a Read Status Enhanced (78h) command to select the LUN prior to issuing a Read Cache Sequential (31h) or Read Cache End (3Fh) command for that LUN.

The figure below defines the Conv. Protocol Read Cache Sequential behavior and timings for the beginning of the cache operations subsequent to a Read command being issued to the target. SR[6] conveys whether the next selected page can be read from the page register:

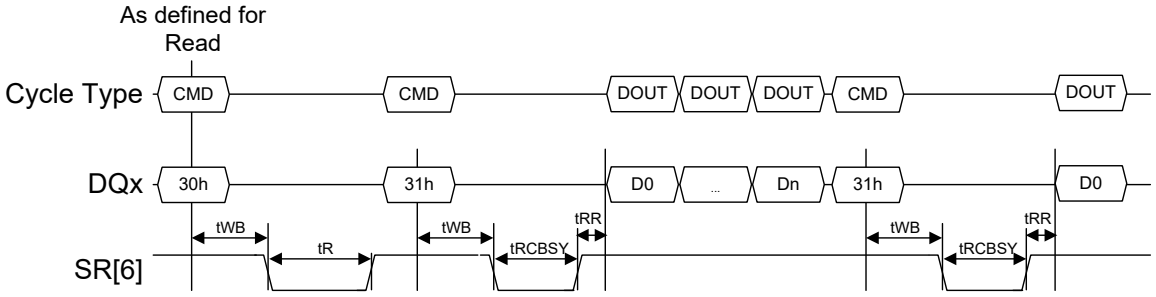


Figure 6-14 Conv. Protocol Read Cache Sequential Timing, Start of Cache Operations

D0-Dn Data bytes/words read from page requested by the original Read or the previous cache operation.

The figure below defines the Conv. Protocol Read Cache Random behavior and timings for the beginning of the cache operations subsequent to a Read command being issued to the target. SR[6] conveys whether the next selected page can be read from the page register:

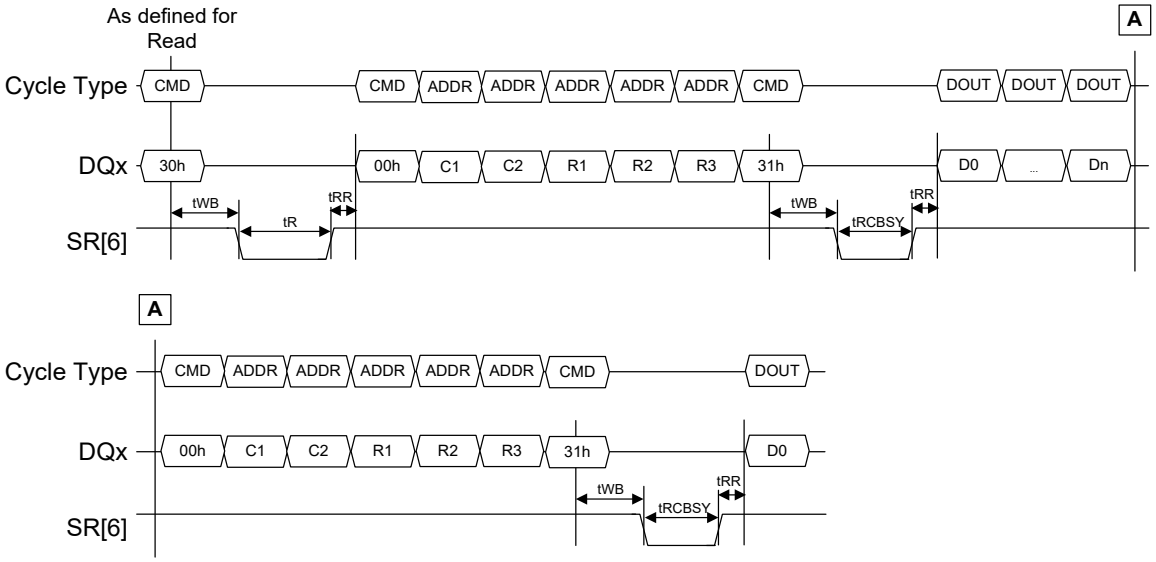


Figure 6-15 Conv. Protocol Read Cache Random Timing, Start of Cache Operations

C1-C2 Column address of the page to retrieve. C1 is the least significant byte. The column address is ignored.

R1-R3 Row address of the page to retrieve. R1 is the least significant byte.

D0-Dn Data bytes/words read from page requested by the original Read or the previous cache operation

The figure below defines the Conv. Protocol Read Cache (Sequential or Random) behavior and timings for the end of cache operations. This applies for both Read Cache Sequential and Read Cache Random. A command code of 3Fh indicates to the target to transfer the final selected page into the page register, without beginning another background read operation. SR[6] conveys whether the next selected page can be read from the page register:

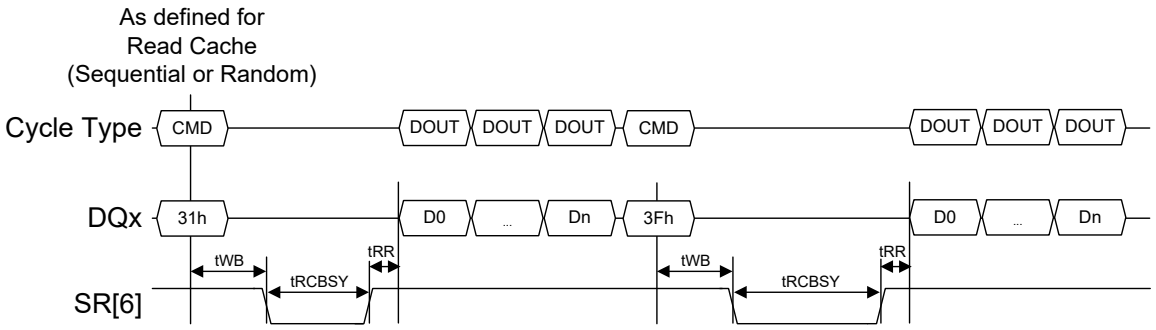


Figure 6-16 Conv. Protocol Read Cache Timing, End of Cache Operations

D0-Dn Data bytes/words read from page requested by the previous cache operation.

6.16. Page Program Definition

The Page Program command transfers a page or portion of a page of data identified by a column address to the page register. The contents of the page register are then programmed into the Flash array at the row address indicated. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero.

The figure below defines the Conv. Protocol Page Program behavior and timings. Writing beyond the end of the page register is undefined.

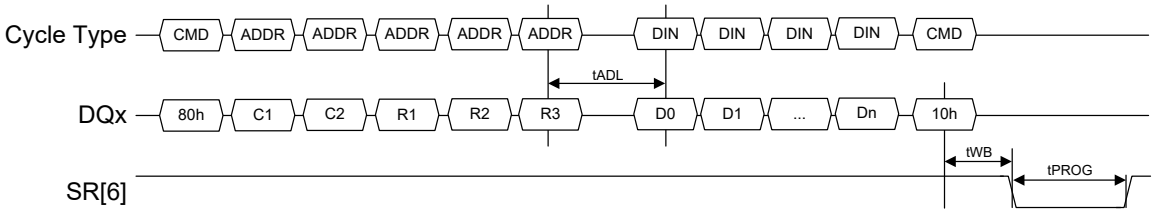


Figure 6-17 Conv. Protocol Page Program Timing

C1-C2 Column address of the starting buffer location to write data to. C1 is the least significant byte.

R1-R3 Row address of the page being programmed. R1 is the least significant byte.

D0-Dn Data bytes/words to be written to the addressed page.

6.17. Page Cache Program Definition

The Page Cache Program function permits a page or portion of a page of data to be written to the Flash array for the specified LUN in the background while the next page to program is transferred by the host to the page register.

Figure 6-18, Figure 6-19, and Figure 6-20 define the Conv. Protocol Page Cache Program behavior and timings.

The 10h command may be used to end the Page Cache Program sequence. After the 10h command is issued, all data is written to the Flash array prior to when SR[5] (ARDY) and SR[6] (RDY) transition from zero to one within tPROG time (see Figure 6-19).

The 15h command may also be used to end the Page Cache Program sequence. If a 15h command is used to end the Page Cache Program sequence, SR[6] (RDY) transitions from zero to one within tPCBSY time, but SR[5] (ARDY) transitions from zero to one within tPROG time (see Figure 6-20).

NAND devices may support both or only one of 10h and 15h commands to end the Page Cache Program Sequence. Please refer to the vendor datasheet for information on what Page Cache Program sequence ending command/s is/are supported by a device.

SR[0] (FAIL) is valid after SR[5] (ARDY) transitions from zero to one until the next transition.
SR[1] (FAILC) is valid after SR[6] (RDY) transitions from zero to one, and this is not the first operation.

Note that tPROG at the end of the caching operation may be longer than typical as this time also accounts for completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

If the program page register clear enhancement is supported, then the host may choose to only clear the page register for the selected LUN and plane address when a Program (80h) command is received. Refer to FA01h register table for details on this feature.

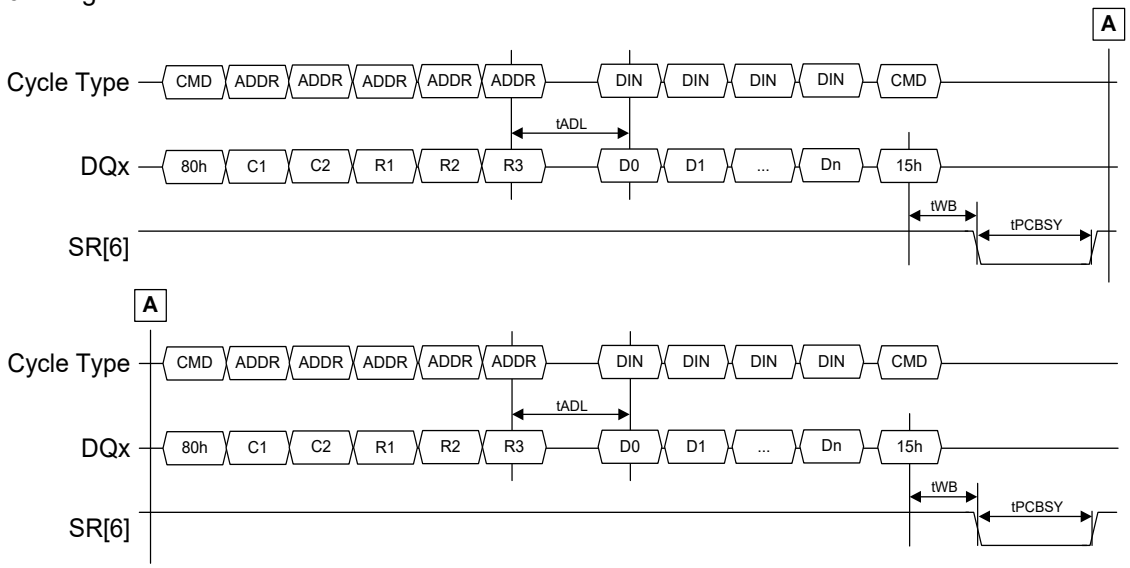


Figure 6-18 Conv. Protocol Page Cache Program Timing, Start of Operations

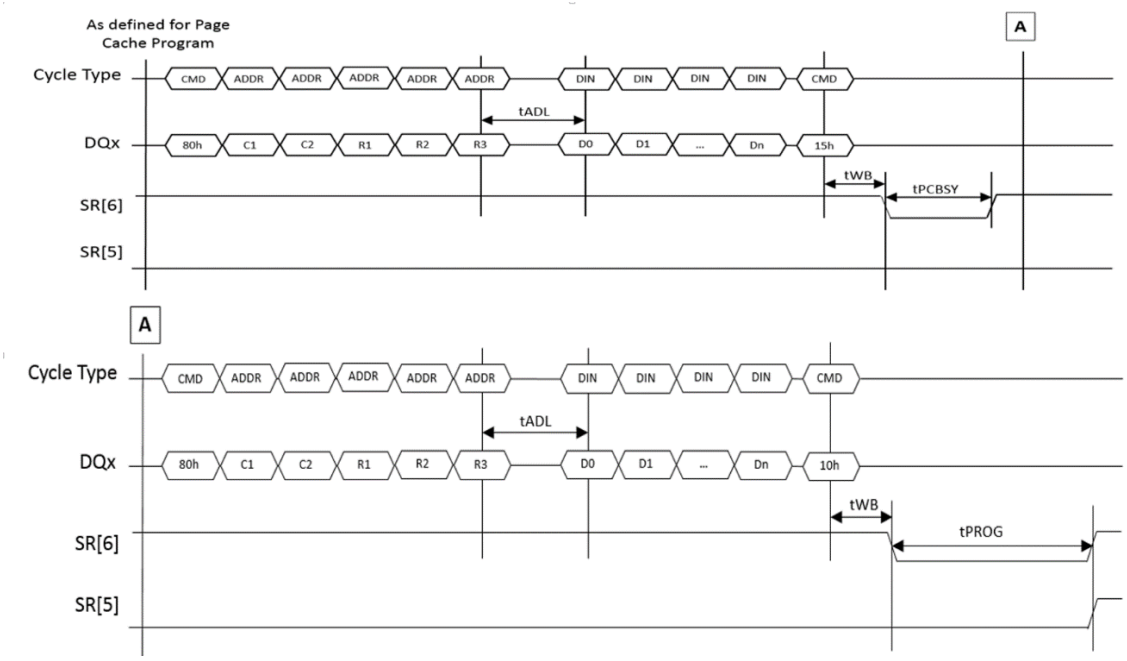


Figure 6-19 Conv. Protocol Page Cache Program Timing, End of Operations using 10h

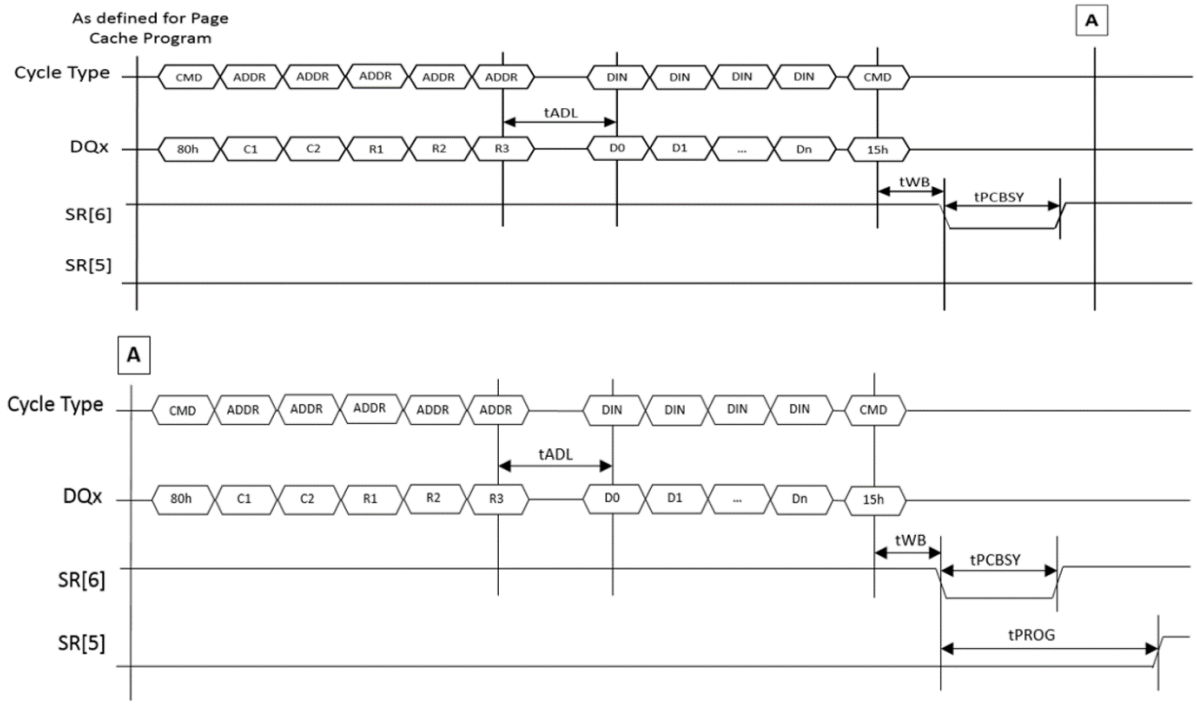


Figure 6-20 Conv. Protocol Page Cache Program Timing, End of Operations using 15h

C1-C2 Column address of the starting buffer location to write data to. C1 is the least significant byte.

R1-R3 Row address of the page being programmed. R1 is the least significant byte.

D0-Dn Data bytes/words to be written to the addressed page.

6.18. Copyback Definition

The Copyback function reads a page of data from one location on a LUN and then moves that data to a second location on the same LUN. The data read from the first location may be read out by the host using Change Read Column or Change Read Column Enhanced commands. The host may then perform data modification using Change Write Column or Change Row Address commands as needed, and then complete programming of the data to the second location on the LUN with a Copyback Program sequence.

The figure below defines the Conv. Protocol Copyback behavior and timings.

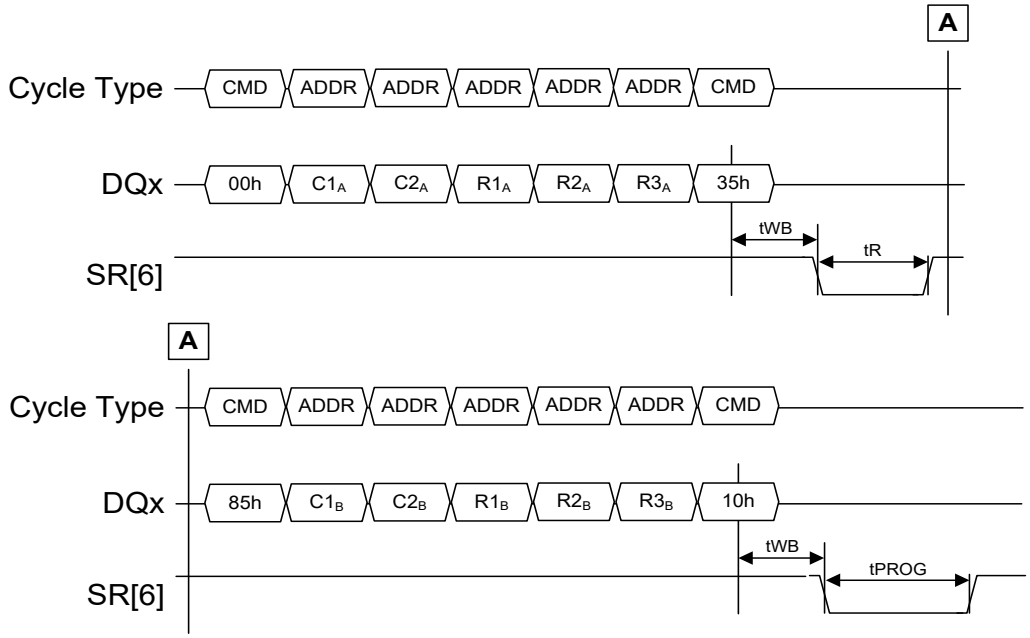


Figure 6-21 Conv. Protocol Copyback Timing

$C1_A$-$C2_A$	Column address of the page to retrieve. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$	Row address of the page to retrieve. $R1_A$ is the least significant byte.
$C1_B$-$C2_B$	Column address of the page to program. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$	Row address of the page to program. $R1_B$ is the least significant byte.

Copyback uses a single page register for the read and program operation.

When multi-plane addressing is supported, the multi-plane address for Copyback Read and Copyback Program for a non-multi-plane Copyback operation shall be the same.

Copyback may also have odd/even page restrictions. Specifically, when reading from an odd page, the contents may need to be written to an odd page. Alternatively, when reading from an even page, the contents may need to be written to an even page. Refer to section 6.7.1.3.

Figure 6-22 and Figure 6-23 show the Conv. Protocol Copyback sequence with data output and data modification.

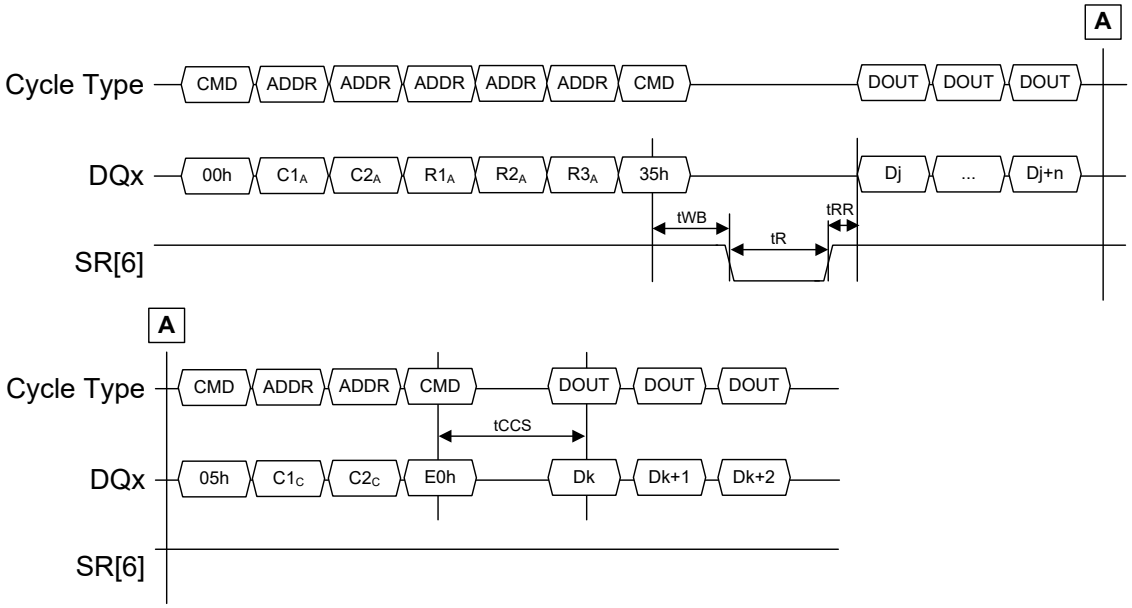


Figure 6-22 Conv. Protocol Copyback Read with Data Output

NOTE: NAND vendors may require the use of Change Read Column Enhanced command and disallow the use of Change Read Column command when outputting data from the NAND page register (see vendor datasheet).

C1 $_A$-C2$_A$ Column address of the page to retrieve. C1$_A$ is the least significant byte.

R1 $_A$-R3$_A$ Row address of the page to retrieve. R1$_A$ is the least significant byte.

Dj-(Dj+n) Data bytes read starting at column address specified in C1-C2$_A$.

C1 $_C$-C2$_C$ Column address of new location (k) to read out from the page register. C1$_C$ is the least significant byte.

Dk-Dk+n Data bytes read starting at column address specified in C1-C2$_C$.

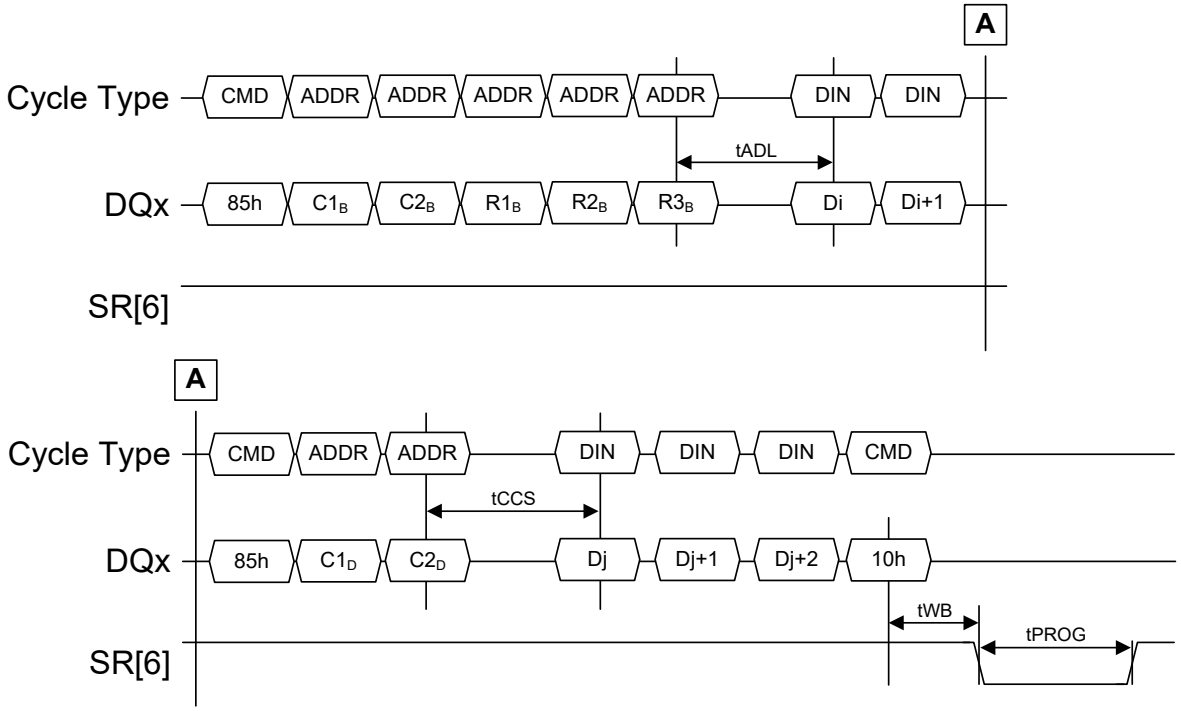


Figure 6-23 Conv. Protocol Copyback Program with Data Modification

$C1_B$-$C2_B$	Column address of the page to program. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$	Row address of the page to program. $R1_B$ is the least significant byte.
Di-Di+n	Data bytes overwritten in page register starting at column address specified in C1-$C2_B$.
$C1_D$-$C2_D$	Column address of new location (j) to overwrite data at in the page register. $C1_D$ is the least significant byte.
Dj-Dj+n	Data bytes overwritten starting at column address specified in C1-$C2_D$

6.19. Small Data Move

Small Data Move is an optional feature for the NAND that allows the host to transfer data to the page register in increments that are less than the page size of the device for both Program and Copyback operations (including multi-plane Program and Copyback operations).

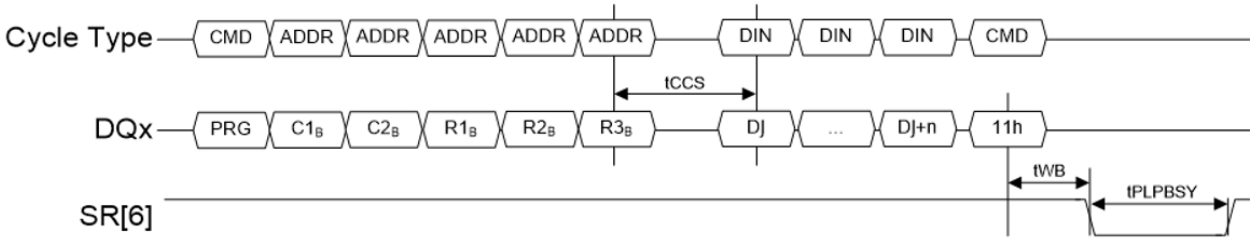


Figure 6-24 Conv. Protocol Small Data Move Sequence

NOTES:
1. NAND vendors may require the use of Change Read Column Enhanced command and disallow the use of Change Read Column command when outputting data from the NAND page register (see vendor datasheet).
2. NAND vendors may remove tPLPBSY busy time, keeping SR[6] HIGH, and instead require the host to provide a vendor specific fixed delay between the 11h command and the next command (see vendor datasheet).

PRG	Program command, either 80h or 85h. Following any data output, the command shall be 85h.
C1-C2$_B$	Column address to write to in the page register. C1$_B$ is the least significant byte.
R1-R3$_B$	Row address of the page to program. R1$_B$ is the least significant byte.
Dj-(Dj+n)	Data bytes to update in the page register starting at column address specified in C1-C2$_B$.

This sequence may be repeated as necessary to complete the data transfer. The row address (R1$_B$ – R3$_B$) shall be the same for all program portions of the sequence destined for the same plane address. The function of the 11h command in a Small Data Move operation is to flush any internal data pipeline in the device prior to resuming data output.

The host may also perform data read outs interleaved with Small Data Move operations. The figure below shows an example in the Conv. Protocol of a Change Read Column sequence to read out data from the LUN interleaved after a Small Data move operation:

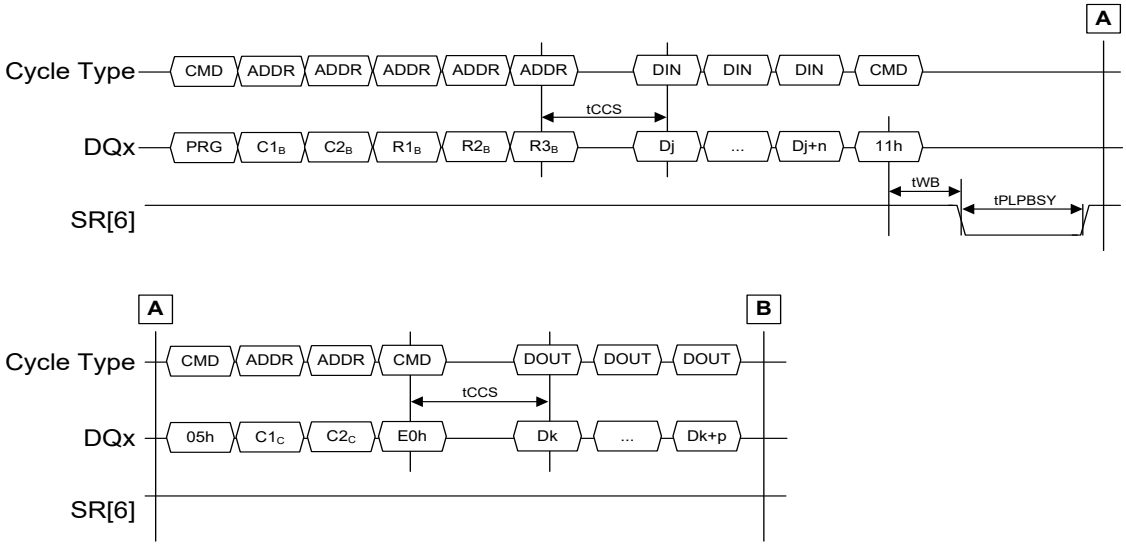


Figure 6-25 Conv. Protocol Small Data Moves with Data Read Out

NOTES:

1. NAND vendors may require the use of Change Read Column Enhanced command and disallow the use of Change Read Column command when outputting data from the NAND page register (see vendor datasheet).

The figure below shows the final program operation in the Conv. Protocol used to complete the Program or Copyback Program sequence:

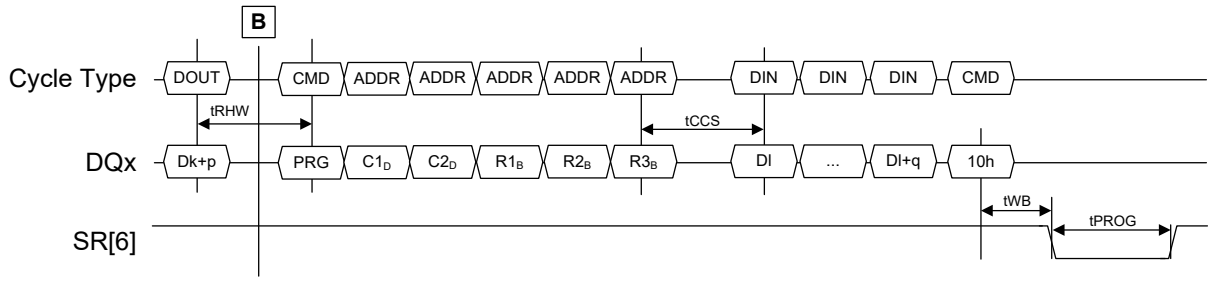


Figure 6-26 Conv. Protocol Small Data Moves, End

PRG	Program command, either 80h or 85h. 85h shall be used if there is any data output as part of the command.
C1-$C2_D$	Column address to write to in the page register. $C1_D$ is the least significant byte.
R1-$R3_B$	Row address of the page to program. $R1_B$ is the least significant byte.
Dl-(Dl+q)	Data bytes to update in the page register starting at column address specified in C1-$C2_D$.

6.20. Change Read Column Definition

The Change Read Column function changes the column address from which data is being read in the page register for the selected LUN. Change Read Column shall only be issued when the LUN is in a read idle condition.

The figure below defines the Conv. Protocol Change Read Column behavior and timings:

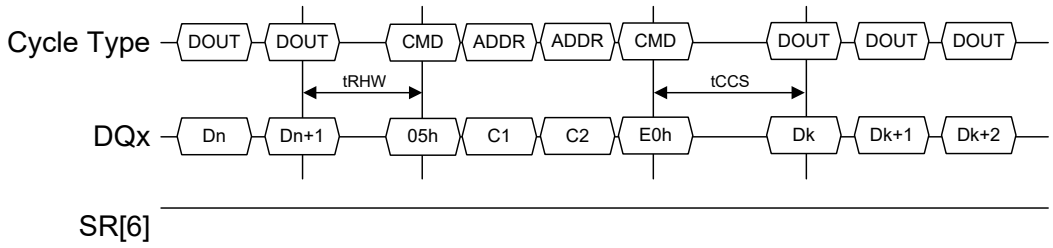


Figure 6-27 Conv. Protocol Change Read Column Tming

Dn Data bytes read prior to the column address change.

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

Dk Data bytes being read starting with the new addressed column.

The host shall not read data out from the LUN until tCCS after the E0h command was issued to the LUN.

NAND vendors may require the use of Change Read Column Enhanced command and disallow the use of Change Read Column command when outputting data from the NAND page register. The use of Change Read Column, however, may still be required for Read Parameter Page, Read Unique ID, and other vendor specific sequences (see vendor datasheet).

6.21. Change Read Column Enhanced Definition

The Change Read Column Enhanced function changes the LUN address, plane address and column address from which data is being read in a page previously retrieved with the Read command. This command is used when independent LUN operations or multi-plane operations are being performed such that the entire address for the new column needs to be given.

The figure below defines the Conv. Protocol Change Read Column Enhanced behavior and timings:

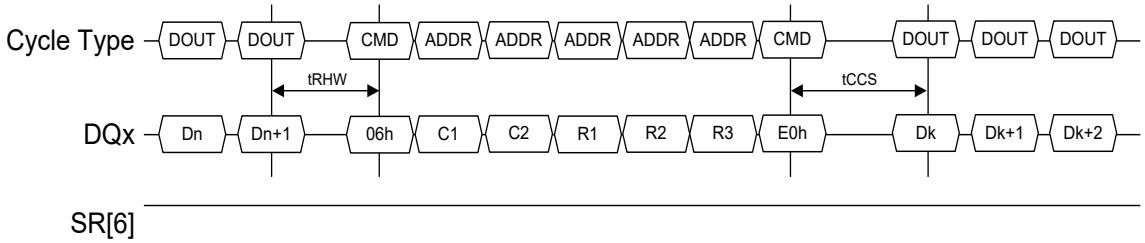


Figure 6-28 Conv. Protool Change Read Column Enhanced Timing

Dn Data bytes read prior to the row and column address change.

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

R1-R3 New row address to be set for subsequent data transfers. R1 is the least significant byte.

Dk Data bytes being read starting with the new addressed row and column.

Change Read Column Enhanced shall not be issued while Target level data output commands (Read ID, Read Parameter Page, Read Unique ID, Get Features) are executing or immediately following Target level commands.

Change Read Column Enhanced causes idle LUNs (SR[6] = 1b) that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Change Read Column Enhanced command responds to subsequent data output. If unselected LUNs are active (SR[6] = 0b) when Change Read Column Enhanced is issued, then the host shall issue a Read Status Enhanced (78h) command prior to subsequent data output to ensure all LUNs that are not selected turn off their output buffers.

The ONFI-JEDEC Joint Taskgroup has defined a modified version of Change Read Column Enhanced, often referred to as Random Data Out. In this definition, a 00h command is given to specify the row address (block and page) for the data to be read, and then a normal Change Read Column command is issued to specify the column address as shown in the figure below. Refer to the NAND vendor datasheet to determine if the device supports this version.

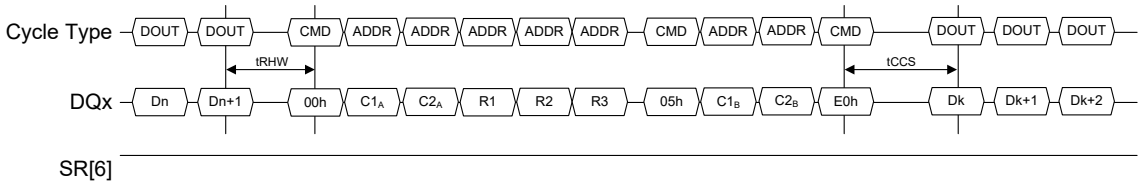


Figure 6-29 Conv. Protocol Change Read Column Enhanced Timing, ONFI-JEDEC Joint Taskgroup Primary Definition

Dn Data bytes read prior to the row and column address change.

$C1_A$-$C2_A$ Column address specified as part of 00h sequence; not used. $C1_A$ is the least significant byte.

R1-R3 New row address to be set for subsequent data transfers. R1 is the least significant byte.

$C1_B$-$C2_B$ New column address to be set for subsequent data transfers. $C1_B$ is the least significant byte.

Dk Data bytes being read starting with the new addressed row and column.

6.22. Change Write Column Definition

The Change Write Column function changes the column address being written to in the page register for the selected LUN.

The figure below defines the Conv. Protocol Change Write Column behavior and timings:

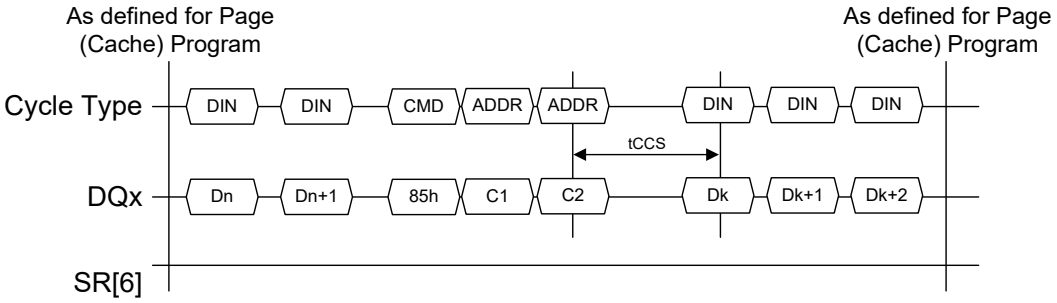


Figure 6-30 Conv. Protocol Change Write Column Timing

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

Dn Data bytes being written to previous addressed column

Dk Data bytes being written starting with the new addressed column

The host shall not write data to the LUN until tCCS after the last column address was written to the LUN.

NAND Vendors may require the host to issue an 11h to end the ongoing data input burst first, wait either tPLPBSY time or a vendor specific fixed delay prior to issuing the Change Write Column command (see vendor datasheet).

6.23. Change Row Address Definition

The Change Row Address function changes the row and column address being written to for the selected LUN. This mechanism may be used to adjust the block address, page address, and column address for a Program that is in execution. The LUN and plane address shall be the same as the Program that is in execution.

The figure below defines the Conv. Protocol Change Row Address behavior and timings:

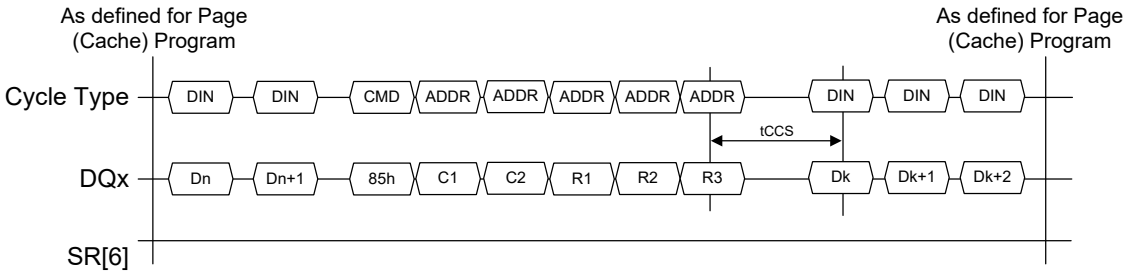


Figure 6-31 Conv. Protocol Change Row Address Timing

C1-C2 New column address to be set for subsequent data transfers. C1 is the least significant byte.

R1-R3 Row address of the page being programmed. The LUN address and plane address shall be the same as the Program in execution. R1 is the least significant byte.

Dn Data bytes being written prior to row address change; will be written to new row address

Dk Data bytes being written to the new block and page, starting with the newly addressed column

NOTE: NAND Vendors may require the host to issue an 11h to end the ongoing data input burst first, wait either tPLPBSY time or a vendor specific fixed delay prior to issuing the Change Row Address command (see vendor datasheet).

The host shall not write data to the LUN until tCCS after the last row address was written to the LUN.

6.24. Volume Select Definition (Conv. Protocol Only)

The Volume Select command is used in the Conv. Protocol to select a particular Volume based on the address specified. Volume Select is required to be used when CE_n pin reduction is used or when matrix termination is used.

The figure below defines the Conv. Protocol Volume Select command sequence behavior and timings:

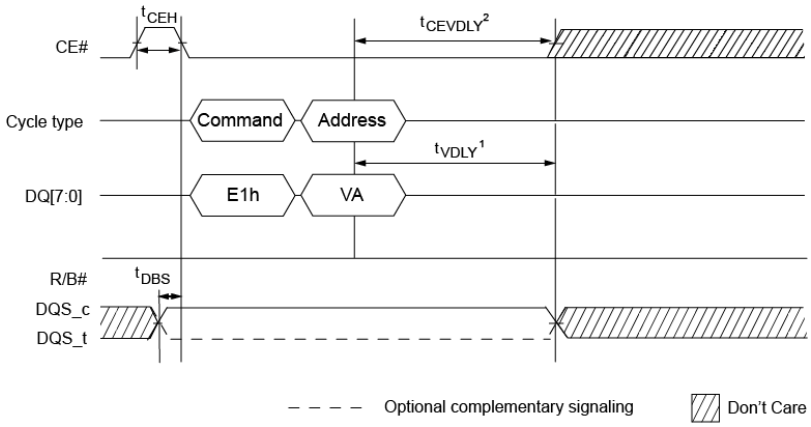


Figure 6-32 Conv. Protocol Volume Select Timing Diagram

Notes:

1. The host shall not issue new commands to any LUN on any Volume until after tVDLY. This delay is required to ensure the appropriate Volume is selected for the next command issued. During a data input operation, Volume Select command may be issued prior to the 10h, 11h, or 15h command if the next command to the Volume in data input mode is Change Row Address. In this case, the host shall wait tCCS before issuing the Change Row Address command.
2. The host shall not bring CE_n high on any Volume until after tCEVDLY. This delay is required to ensure the appropriate Volume is selected based on the previously issued Volume Select command.

The table below defines the Volume Address field specified as part of the command:

Volume Address	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VA	Reserved (0)				Volume Address			

Table 6-7 Volume Address Field Definition

Volume Address Specifies the Volume to select.

The Volume Select command is accepted by all NAND Targets that are connected to a particular Host Target. The command may be executed with any LUN on the Volume in any state. The Volume Select command may only be issued as the first command after CE_n is pulled low; CE_n shall have remained high for tCEH in order for the Volume Select command to be properly received by all NAND Targets connected to the Host Target. DQS (DQS_t) shall remain high for the entire Volume Select command sequence.

When the Volume Select command is issued, all NAND Targets that have a Volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE_n pulled high). If one of the LUNs in an unselected Volume is an assigned terminator for the selected Volume, then that LUN will enter the Sniff state. Refer to Table 4-24 for a description of LUN states for matrix termination.

If the Volume address specified does not correspond to any appointed volume address, then all NAND Targets shall be deselected until a subsequent Volume Select command is issued. If the Volume Select command is not the first command issued after CE_n is pulled low, then the NAND Targets revert to their previously selected, deselected, or sniff states (volume reversion).

6.25. ODT Configure Definition (Conv. Protocol Only)

The ODT Configure command is used to configure on-die termination when using matrix termination. Specifically, ODT Configure specifies whether a particular LUN is a terminator for a Volume(s) and the Rtt settings. If the LUN is specified as a terminator for one or more Volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the Volume(s) it is acting as a terminator for.

The figure below defines the Conv. Protocol ODT Configure behavior and timings:

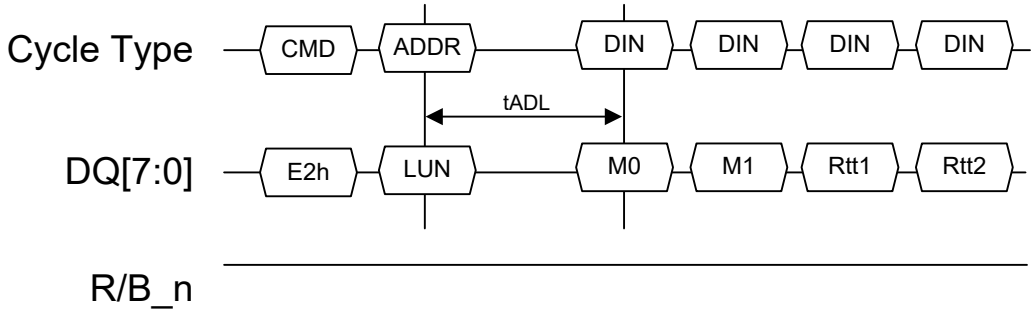


Figure 6-33 Conv. Protocol ODT Configure Timing Diagram

LUN	Specifies the LUN that acts as a terminator. This field is formatted in the same manner as the row address byte that contains the LUN address. Refer to section 3.1. Note that the LUN address may require more than one address cycle if the LUN address spans more than one row address byte. See vendor device datasheet for the number of LUN address cycles needed for this command.
M0	Lower byte of the ODT configuration matrix.
M1	Upper byte of the ODT configuration matrix.
Rtt1	Termination settings for DQ[7:0]/DQS.
Rtt2	Termination settings for RE_n
R	Reserved (0h)

When issuing ODT Configure, each data byte is transmitted twice. The device shall only latch one copy of each data byte. See section 4.3.

The table below defines the M0 and M1 parameters for the command. If a bit is set to one in these parameters, then the LUN shall act as the terminator for the corresponding Volume (Vn) where n corresponds to the Volume address.

Parameter	7	6	5	4	3	2	1	0
M0	V7	V6	V5	V4	V3	V2	V1	V0
M1	V15	V14	V13	V12	V11	V10	V9	V8

Table 6-8 ODT Configure M0 and M1 Parameter Definition

The table below defines Rtt1 and Rtt2 parameters for the command:

Rtt Settings	7	6	5	4	3	2	1	0
Rtt1	DQ[7:0]/DQS/DBI Rtt & ODT Enable for Data Output				DQ[7:0]/DQS/DBI Rtt & ODT Enable for Data Input			
Rtt2	Reserved				RE_n Rtt & ODT Enable			

Table 6-9 ODT Configure Rtt1 and Rtt2 Parameter Definition

DQ[7:0]/DQS/DBI Rtt & ODT Enable for Data Input

This field controls the on-die termination settings for the DQ[7:0], DQS_t and DQS_c signals for data input operations (i.e. writes to the device).

The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh Reserved

DQ[7:0]/DQS/DBI Rtt & ODT Enable for Data Output

This field controls the on-die termination settings for the DQ[7:0], DQS_t and DQS_c signals for data output operations (i.e. reads from the device).

The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh Reserved

RE_n Rtt & ODT Enable

This field controls the on-die termination settings for the RE_t and RE_c signals.

The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh Reserved

When this command is issued, then the updated termination settings take effect immediately. The host should take care when modifying these settings to avoid any signal integrity issues. If issues occur after, then it is recommended to transition to a slower timing mode, make the appropriate updates to the termination settings, and then transition back to the faster timing mode.

The on-die termination settings are retained across all reset commands, including Reset (FFh).

6.26. ODT Disable/Enable (Conv. Protocol Only)

ODT termination causes signal swing on the channel to be smaller than that of an unterminated channel. The NAND and controller internal VrefQ, however, can still be at an untrained state and the smaller signal swing with ODT can cause failure of Set Feature or Read Status and Get Feature sequences. The ODT Disable (1Bh) and ODT Enable (1Ch) commands allow the host to disable and enable the ODT on the NAND via command cycles to work around such limitations.

NAND devices and host shall support ODT disable and enable using using 1Bh/1Ch commands.

- 1Bh disables target and non-target ODT operations
- 1Ch enables target and non-target ODT operations

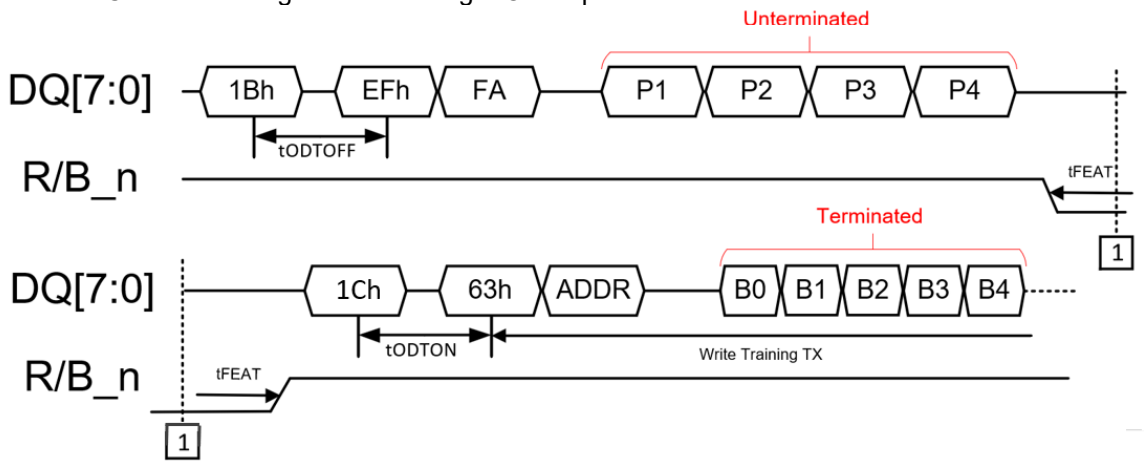


Figure 6-34 Conv. Protocol ODT Disable/Enable Timing

6.27. ZQ Calibration Long

The ZQ CALIBRATION LONG (ZQCL) command is used to perform the initial calibration during a power-up initialization or reset sequence. Writing F9h to the command register, followed by one row address cycle containing the LUN address performs ZQCL on the selected die. This command may be issued at any time by the controller, depending on the system environment. The ZQCL command triggers the calibration engine inside the NAND. After calibration is achieved, the calibrated values are transferred from the calibration engine to the NAND I/O, which are reflected as updated RON and Rtt values.

During ZQCL operation, no array operations are allowed on the NAND device that is performing the ZQCL operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCL operation.

The NAND is allowed a timing window defined by tZQCL to perform a full calibration and transfer of values. When ZQCL is issued the timing parameter tZQCL must be satisfied.

When ZQCL operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should check the RZQ resistor connection. If the ZQCL operation fails, the device will revert to a vendor specific value. If RESET operation is executed during the ZQCL operation, the NAND device will revert to factory settings for output driver strength and ODT values (e.g. as if no ZQ calibration was performed).

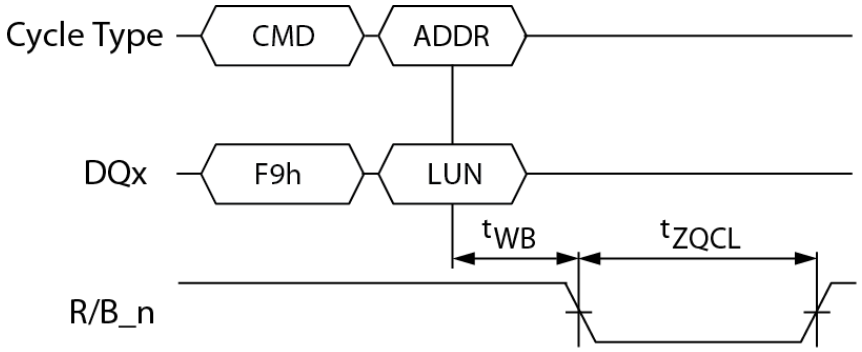


Figure 6-35 Conv. Protocol ZQ Calibration Long

6.28. ZQ Calibration Short

The ZQ CALIBRATION SHORT (ZQCS) command is used to perform periodic calibration to account for small voltage and temperature variations. Writing D9h to the command register, followed by one row address cycles containing the LUN address, performs ZQCS on the selected die. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter tZQCS. A ZQCS command can effectively correct a minimum of 1.5% RON and Rtt impedance error within tZQCS.

During ZQCS operation, no array operations are allowed on the NAND device that is performing the ZQCS operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCS operation.

When ZQCS operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should follow vendor specific instructions. If the ZQCS operation fails, the device will revert to a vendor specific value.

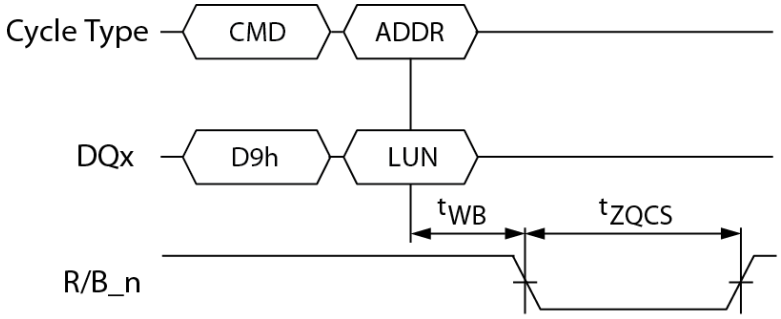


Figure 6-36 Conv. Protocol ZQ Calibration Short

6.29. Set Features Definition

The Set Features function modifies the settings of a particular feature. For example, this function can be used to enable a feature that is disabled at power-on.

The figure below defines the Conv. Protocol Set Features behavior and timings:

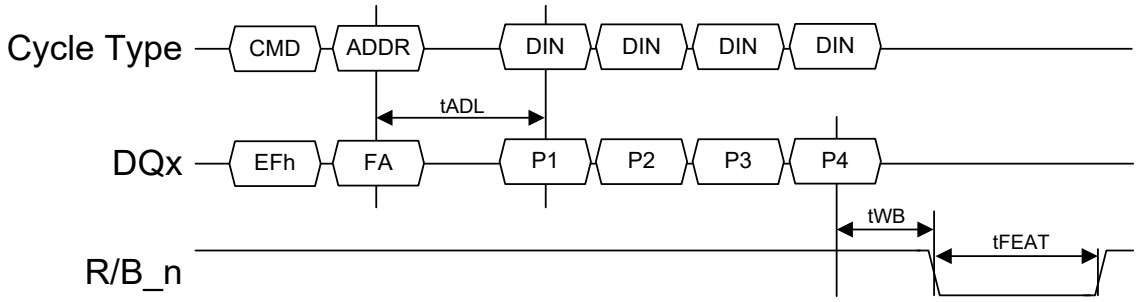


Figure 6-37 Conv. Protocol Set Features Timing

NOTE: NAND vendors may opt to keep the busy signal high, requiring a vendor specific fixed delay time instead. Refer to vendor device datasheet.

FA Feature address identifying feature to modify settings for.

P1-P4 Parameters identifying new settings for the feature specified.

P1 Sub feature parameter 1
P2 Sub feature parameter 2
P3 Sub feature parameter 3
P4 Sub feature parameter 4

Refer to section 8 for the definition of features and sub feature parameters.

When issuing Set Features, each data byte is transmitted twice. The device shall only latch one copy of each data byte (see section 4.3).

The LUN Set Features (D5h) command functions the same as the target-level Set Features (EFh) command except only the addressed LUNs settings are modified. It shall be assumed that wherever Set Features command is mentioned in this document that LUN Set Features functions the same except where differences are explicitly stated.

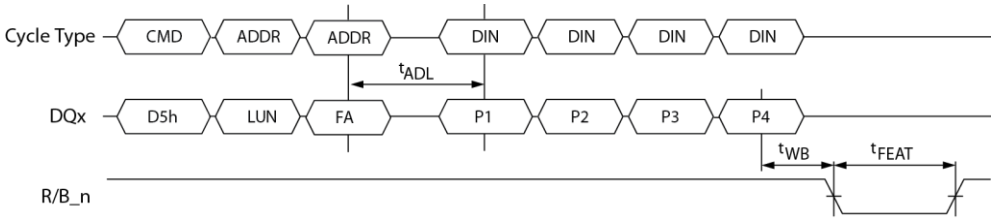


Figure 6-38 Conv. Protocol LUN Set Features Timing

NOTE: NAND vendors may opt to keep the busy signal high, requiring a vendor specific fixed delay time instead. Refer to vendor device datasheet.

LUN LUN Address. LA0 = bit 0, LA1 = bit1, LA2 = bit 2. (i.e. LUN 0 = 00h, LUN 1 = 01h)

FA Feature address identifying feature to modify settings for.

P1-P4 Parameters identifying new settings for the feature specified.

P1 Sub feature parameter 1

P2 Sub feature parameter 2
P3 Sub feature parameter 3
P4 Sub feature parameter 4

6.30. Get Features Definition

The Get Features function is the mechanism the host uses to determine the current settings for a particular feature. This function shall return the current settings for the feature (including modifications that may have been previously made with the Set Features function).

The figure below defines the Conv. Protocol Get Features behavior and timings:

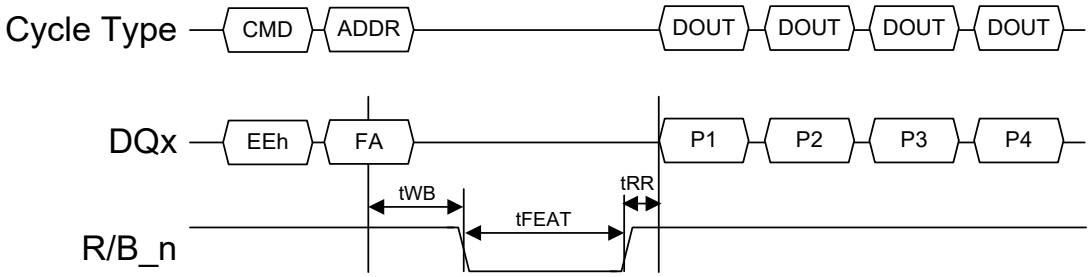


Figure 6-39 Conv. Protocol Get Features Timing

NOTE: NAND vendors may opt to keep the busy signal high, requiring a vendor specific fixed delay time instead. Refer to vendor device datasheet.

FA Feature address identifying feature to return parameters for.

P1-P4 Current settings/parameters for the feature identified by argument P1

P1 Sub feature parameter 1 setting
P2 Sub feature parameter 2 setting
P3 Sub feature parameter 3 setting
P4 Sub feature parameter 4 setting

After reading the first byte of data, the host shall complete reading all desired data before issuing another command (including Read Status or Read Status Enhanced).

When issuing Get Features, each data byte is received twice. The host shall only latch one copy of each data byte. See section 4.3.

If Read Status is used to monitor when the tFEAT time is complete, the host shall issue a command value of 00h to begin transfer of the feature data starting with parameter P1.

The LUN Get Features (D4h) command functions the same as the target level Get Features (EEh) command except only the addressed LUNs settings are returned. It shall be assumed that wherever Get Features command is mentioned in this document that LUN Get Features functions the same except where differences are explicitly stated.

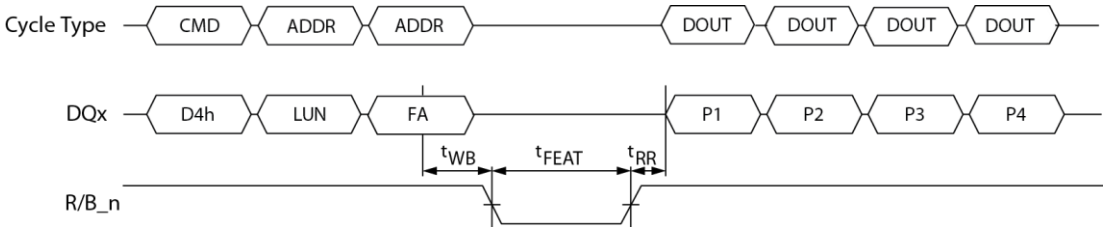


Figure 6-40 Conv. Protocol LUN Get Features Timing

NOTE: NAND vendors may opt to keep the busy signal high, requiring a vendor specific fixed delay time instead. Refer to vendor device datasheet.

LUN LUN Address. LA0 = bit 0, LA1 = bit1, LA2 = bit 2. (i.e. LUN 0 = 00h, LUN 1 = 01h, etc.)

FA Feature address identifying feature to return parameters for.

P1-P4 Current settings/parameters for the feature identified by argument P1

- P1 Sub feature parameter 1 setting
- P2 Sub feature parameter 2 setting
- P3 Sub feature parameter 3 setting
- P4 Sub feature parameter 4 setting

Refer to section 8 for the definition of features and sub feature parameters.

7. Data Training and Monitor Features

7.1. Introduction and Training Flow

This section contains descriptions of different data training and monitoring features that may be supported on ONFI NAND devices.

Refer to the 4.1 Data Interface Overview section for general guidance as to when these features are typically required to support a particular data rata rate.

Refer to the 4.5 Interface Initialization section for general guidance on the recommended initialization and data training flow.

The figure below shows an example of a more detailed data training flow employing the various training features:

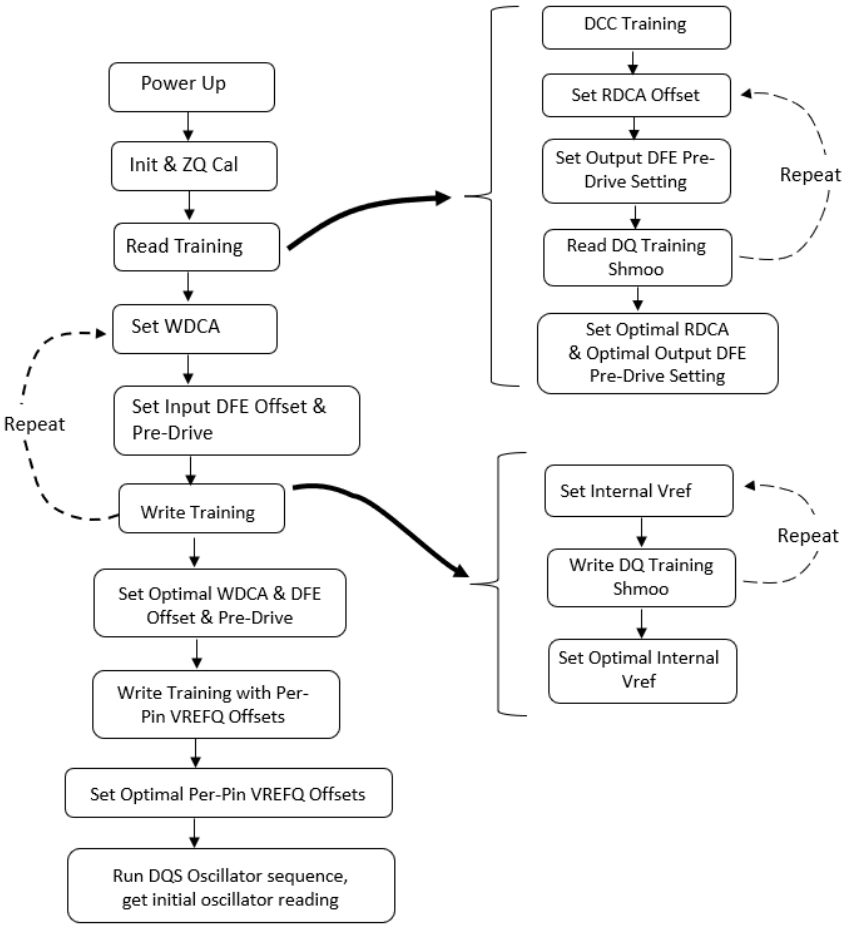


Figure 7-1 Example Data Training Flow

7.2. DCC Training

DCC Training enables the NAND device to compensate for duty cycle mismatch on the RE_t/c signal.

Two types of DCC training are defined: explicit DCC and implicit DCC.

- In Explicit DCC training, the training is performed using a specific command sequence. Explicit DCC training may be initiated via Set Feature or if supported by the NAND vendor, via command (see vendor datasheet).
- In Implicit DCC training, the NAND devices carries out DCC training during warmup cycles. The specific number of warmup cycles is defined in the NAND vendor datasheet.

When performing a status read to read out the pass/fail results of DCC training, since DCC Training is performed before Read DQ Training, it is recommended that the DQS falling edge or the successive DQS rising edge is used to capture the read status data.

7.2.1. Explicit DCC Training using Set Feature

Explicit DCC training using Set Feature is initiated by setting the DCCE_EN enable bit at Feature Address 20h P1[0]. When DCCE_EN is enabled, the DCCI_EN bit at P1[1] becomes a “don’t care”. On power-up, DCCE_EN shall be disabled.

After issuing the Set Feature to enable DCCE_EN, the host shall issue the Random Data Out command with the address information based on the Set Feature command used to enable the DCC training feature and calibrate RE_t and RE_c by sending those signals for a page size. (Page size shall be given by vendor datasheet.). If the Set Feature command used was an EFh command, then the addresses for the Random Data Out command sequence shall be filled with 00h. If the Set Feature command used was the D5h (Set Feature for Each LUN) command, then the addresses for the Random Data Out command sequence must have the same LUN address that was used during the D5h command. If LUN address is not used in the Random Data Out sequence, then fix all column address to “00h”. The host shall then calibrate RE_t and RE_c by sending those signals for a page size. During the data output cycles produced by these RE_t and RE_c toggles, the DQ and DQS of the LUNs under training may be driven or Hi-Z depending on the NAND vendor DCC Training implementation. Refer to the NAND vendor datasheet to see if DQ and DQS are driven or Hi-Z during this time. The data for these data output cycles shall be invalid and ignored by the host. Care should be taken to avoid bus contention during these data output cycles, especially for multi-LUN DCC training cases where the NAND vendor DCC Training implementation drives the DQ and DQS signals.

After sending RE_t and RE_c for page size length, Status Check shall be performed to confirm whether DCC is Pass or Fail via SR[0]. If fail, the host shall issue Random Data Out command and resend RE_t and RE_c signals to calibrate again. If EFh is used, all the LUNs under the Target perform DCC (All LUN DCC). If D5h command is used, selected LUN under the Target performs DCC (Single LUN DCC). The device may support either or both of All LUN DCC and Single LUN DCC. See vendor’s datasheet. After completing Explicit DCC using Set Feature, DCCE_EN shall be set to 0.

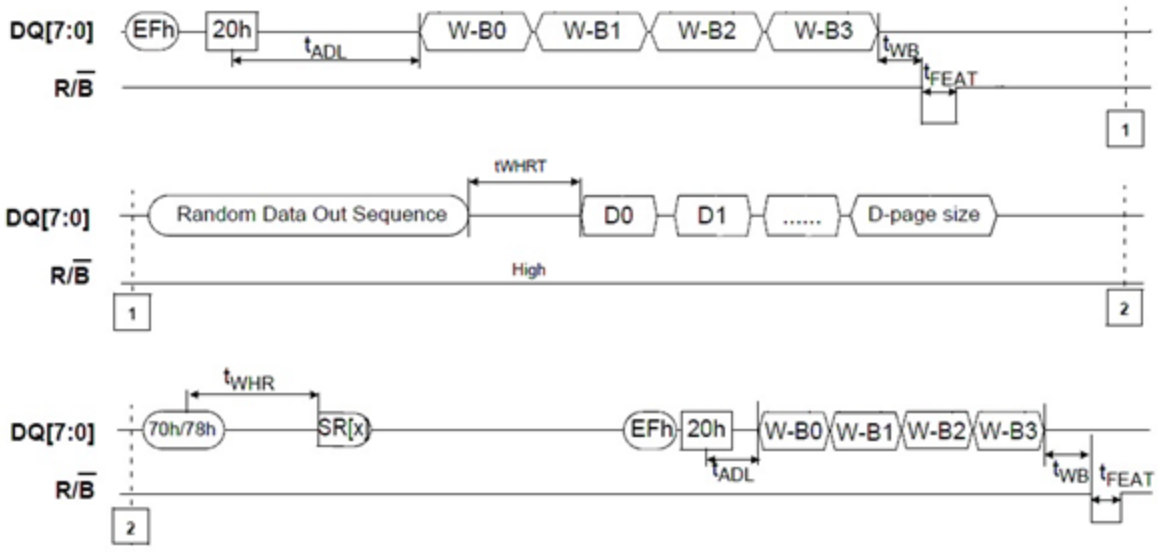


Figure 7-2 DCC Training using Set Feature

7.2.2. Explicit DCC Training using Command (Optional)

Explicit DCC training using a command can be initiated using CMD18h followed by LUN Address. After issuing LUN address, the host shall calibrate RE_t and RE_c by toggling these signals for a page size. (Page size shall be given by vendor datasheet). The data returned by the device is vendor specific data pattern so that there is no impact of data pattern on DCC training. After sending the required number of RE_t and RE_c signals, Status Check shall be performed to confirm whether DCC is Pass or Fail. If status is a Fail, user has to issue RESET command (FFh) wait for the RESET command to execute and then re-issue the Command based DCC sequence.

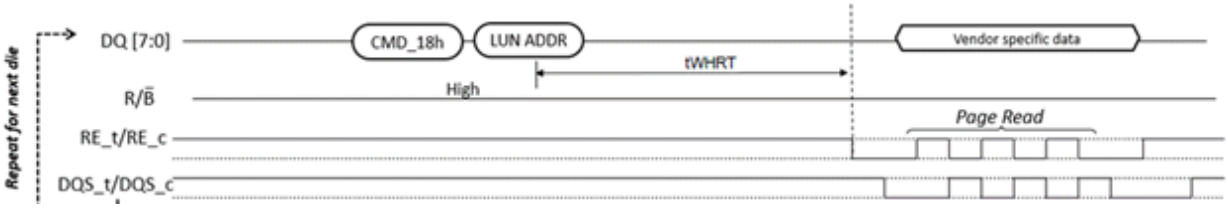


Figure 7-3 DCC (RE_t/c) Training using Command (Optional)

Timing specs of RE_t/RE_c during DCC page read will follow normal Read timing as per vendor datasheet.

7.2.3. Implicit DCC Training

Implicit DCC is an optional feature for the NAND devices to support. It is initiated by the host setting the DCCI_EN bit at Feature Address 20h P1[1]. If DCCI_EN is enabled, the NAND device carries out DCC training to update the training result during warm up cycles where “warm up cycles” is sometimes referred to “DQS latency”. Implicit DCC may require specific number of warm up cycles to be set and it shall be given in the vendor datasheet.

7.3. Read Duty Cycle Adjustment (RDCA)

Read Duty Cycle Adjustment (RDCA) is an optional NAND feature that provides a way for the NAND to compensate input RE_t/c duty cycle distortion. The RDCA feature is recommended to apply for the offset compensation of the duty cycle mismatch after DCC training and is controlled via FA28h.

7.4. Read DQ Training

Read DQ Training is a feature which allows the host to align DQS and DQ signals caused by mismatches in the signal paths.

During Read DQ Training, the NAND outputs a 16-bit user-defined pattern on each of the DQ pins. A total of 16 bytes is outputted by the NAND device, although NAND vendors may optionally provide a 32-byte pattern.

Read DQ Training is initiated by issuing a [Read DQ Training] command 62h followed by LUN Address then three address cycles. Three address cycles are 1st address (8bit invert mask), 2nd address (first eight-bit pattern) and 3rd address (second eight-bit pattern). The following table shows example data pattern (i.e. 1st 35h, 2nd 5Ah, 3rd 82h address).

Pin	Inverse Setting		0~15																16~31 (Optional)															
	(Mask)		1st Input DATA : 5Ah								2nd Input DATA : 82h								Swap 1st,2nd data of DQ4~7 ↔ DQ0~3 (Optional)																
DQ0	1 (Inverse)	35h	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ1	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ2	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ3	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ4	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ5	1 (Inverse)		1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1
DQ6	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0
DQ7	0		0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Figure 7-4 Example of User Defined Pattern for Read DQ Training

If '1' is indicated by a bit in 1st address, DQx corresponding to a bit shall be inverted and the NAND device outputs data pattern designated by 2nd and 3rd addresses masked I/O following in invert mask indicated by 1st address by RE, /RE toggling, the data will be inversed by masked I/O.

If host issue RE, /RE toggling for more than the vendor defined pattern length, data will be wrapped.

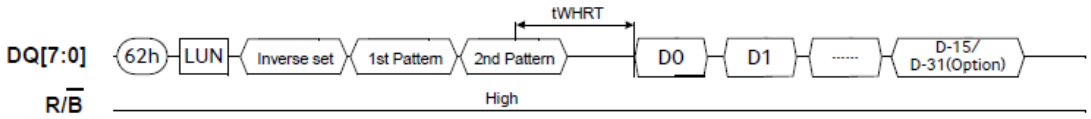


Figure 7-5 Read DQ Training

7.5. Write Duty Cycle Adjustment (WDCA)

Write Duty Cycle Adjustment (WDCA) provides a way for the NAND to compensate for input DQS duty cycle loss at the NAND device.

The controller repeats between configuring NAND WDCA settings and performing Write Training sequence to find the optimum WDCA setting. The tFEAT time for feature address 24h is vendor specific.

7.6. Write Per-Pin VREFQ Offsets

Write Per-Pin VrefQ offsets allow the host to fine-tune internal VrefQ levels on a LUN to compensate for pin-pin timing variation.

The base NAND VrefQ setting is provided by FA23h while FA40h & FA41h provide the pin specific offset information. The final VrefQ setting for a pin is determined by the base setting from FA23h and the offset information from FA40h/41h.

7.7. Decision Feedback Equalizer (DFE)

The NAND Decision Feedback Equalizer (DFE) feature provides a way for the NAND to compensate for data eye aperture shinkage during data input at higher data rates. The DFE feature also provides a way to enable DQ pre-drive behavior during data output.

Feature Address 27h controls DFE feature operations. FA 27h P1[2:0] enables/disables DFE for data input and controls the DFE coefficient. FA 27h P1[5:4] control DQ pre-drive initialization behavior for data input while P1[7:6] control DQ pre-drive behavior for data output.

When DFE for data input is enabled via FA 27h P1[2:0], NAND devices with 1-tap DFE require 2UI DQ pre-drive to 0, in order to precondition DFE circuitry prior to the burst of user data. The pre-drive setting for data input is configured via FA 27h P1[5:4]. Note: Prior to configuring the DFE DQ pre-drive settings for data input in FA 27h, the host must have first configured the number of warmup cycles for data input in FA02h to a setting that is greater than or equal to the number of input pre-drive cycles (1 warmup cycle = 2UI pre-drive).

The figure below shows how DQ signals must be pre-driven to 0 by the controller for 2UI for the 1-tap DFE case and 4UI for the 4-tap DFE case. NAND support for 4-tap DFE is optional. It is vendor specific whether 4UI or 8UI DQ pre-drive to 0 is required when 4-tap DFE is supported.

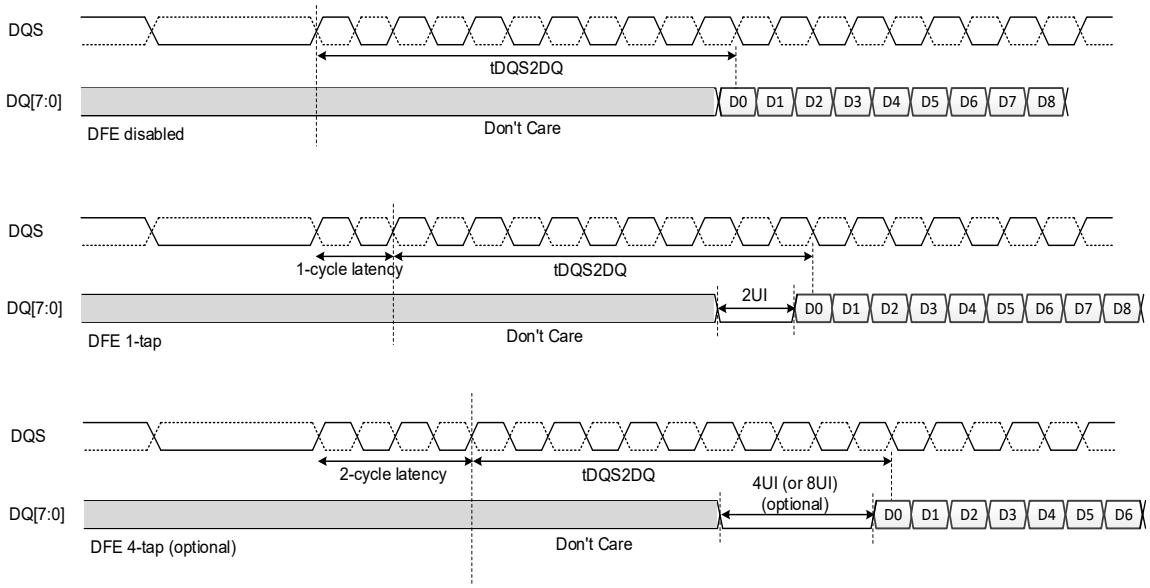


Figure 7-6 DFE DQ Pre-Drive for Data Input Examples

The FA 27h P1[7:6] bits control the DQ output pre-drive from the NAND. DQ output pre-drive forces the NAND to output 0 for a certain number of UI. This is useful in cases where the controller supports DFE and requires the DQ signals to be pre-driven to 0 for DFE circuitry initialization. Note: Prior to configuring the DFE DQ pre-drive settings for data output in FA 27h, the host must have first configured the number of warmup cycles for data output in FA02h to a setting that is greater than or equal to the number of output pre-drive cycles (1 warmup cycle = 2UI pre-drive).

The figure below shows DQ signals being pre-driven by the NAND to 0 for 2UI and 4 UI cases:

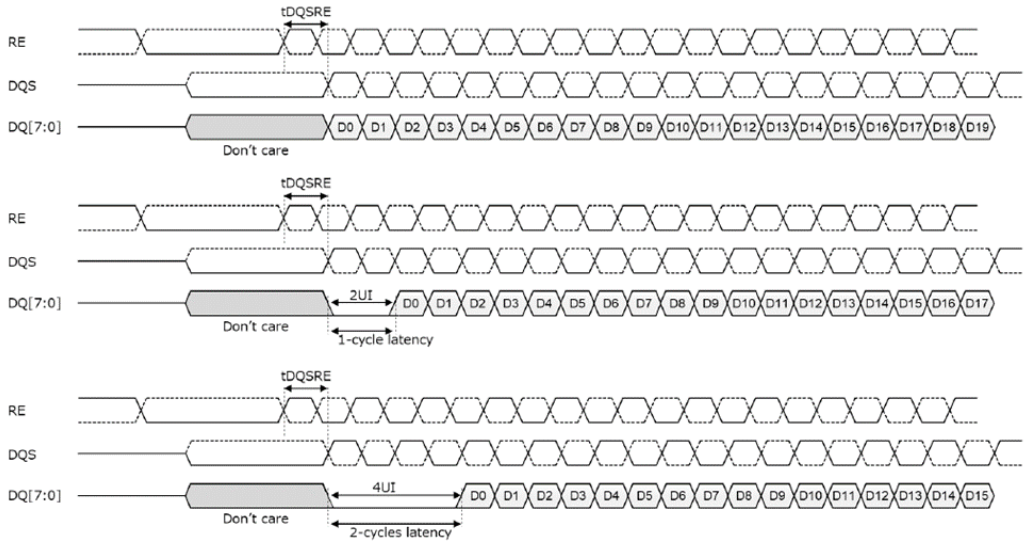


Figure 7-7 DFE Pre-Drive for Data Output

7.8. Write DQ Training (Tx Side)

Write DQ Training (Tx Side) is a training feature which allows the host to align DQS and DQ signals at the NAND latch. With Write DQ Training (Tx Side), host-side delays are tuned to compensate for DQ and DQS path mismatches.

To perform Write training Tx side, the controller shall issue 63h command followed LUN address. After issuing LUN address, the host shall input data pattern and confirm whether the input is successfully done by checking the output by NAND in following sequence.

Data sizes for Write DQ is pre-defined by NAND. The host shall recognize the data sizes by Get Feature (Feature Address = 20h, P3) and shall input and output the data based on the size. If fewer data than pre-defined data bytes are written, then unwritten registers will have un-defined data when read back. If over pre-defined data bytes read were executed, the data are also un-defined and invalid.

After writing data to the NAND with 63h command, the data can be read back with 64h command followed by LUN address and the results shall be compared with “expected” data to see if further training (DQ delay) is needed.

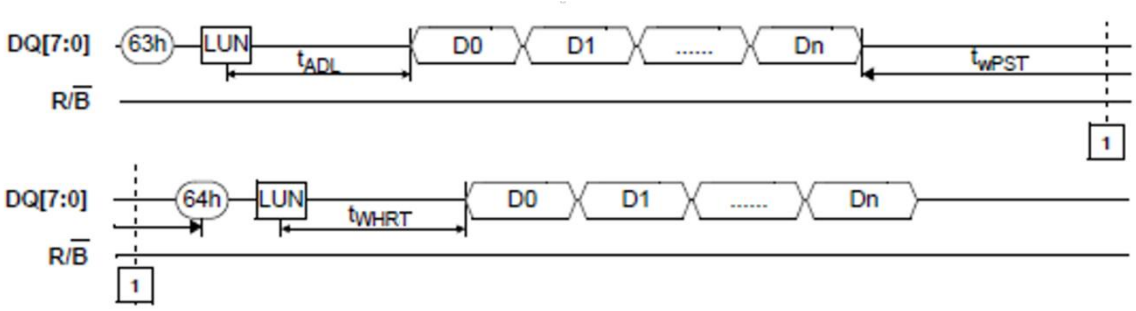


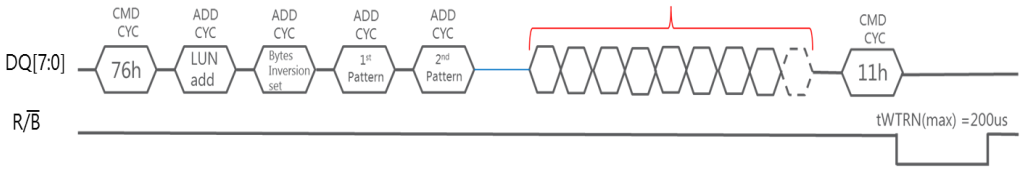
Figure 7-8 Write DQ Training (Tx side)

7.9. Write DQ Training (Rx Side, Optional)

Write DQ Training (Rx Side) is a training feature which allows the host to align DQS and DQ signals at the NAND latch. With Write DQ Training (Tx Side), NAND-side delays are tuned to compensate for DQ and DQS path mismatches.

To perform Write training (Rx Side), the controller shall issue 76h command followed by LUN address. After issuing LUN address, the host shall issue 3 address cycles for data pattern format. The definition of these 3 address cycles are the same as the ones mentioned in read training. After the 3 address cycles, the host shall issue data input with the same pattern determined by the 3 address cycles for 1 full page. The input data shall be wrapped around the data pattern length (16 or 32) until a full-page data is issued. The training sequence shall be ended by 11h command and the NAND will perform write training during the R/B_ time (tWTRN). The host may poll the R/B_ status by status command to check the completion of the training operation. The status of the training for each DQ can be checked by issuing Get Feature by LUN with address 21h (P2 and P3). The complete byte definition is given in the Feature Address 21h table.

DIN Burst



DIN Burst: Data Input with the same pattern specified in 3 address cycle wrapping around the data pattern length (16 or 32) for 1 full page.

Figure 7-9 Write DQ Training (Rx side) Optional

If Write Training (Rx side) passes, then the host may skip Write Training (Tx side).

The following flow chart is an example of the process for doing Write Training (Rx side):

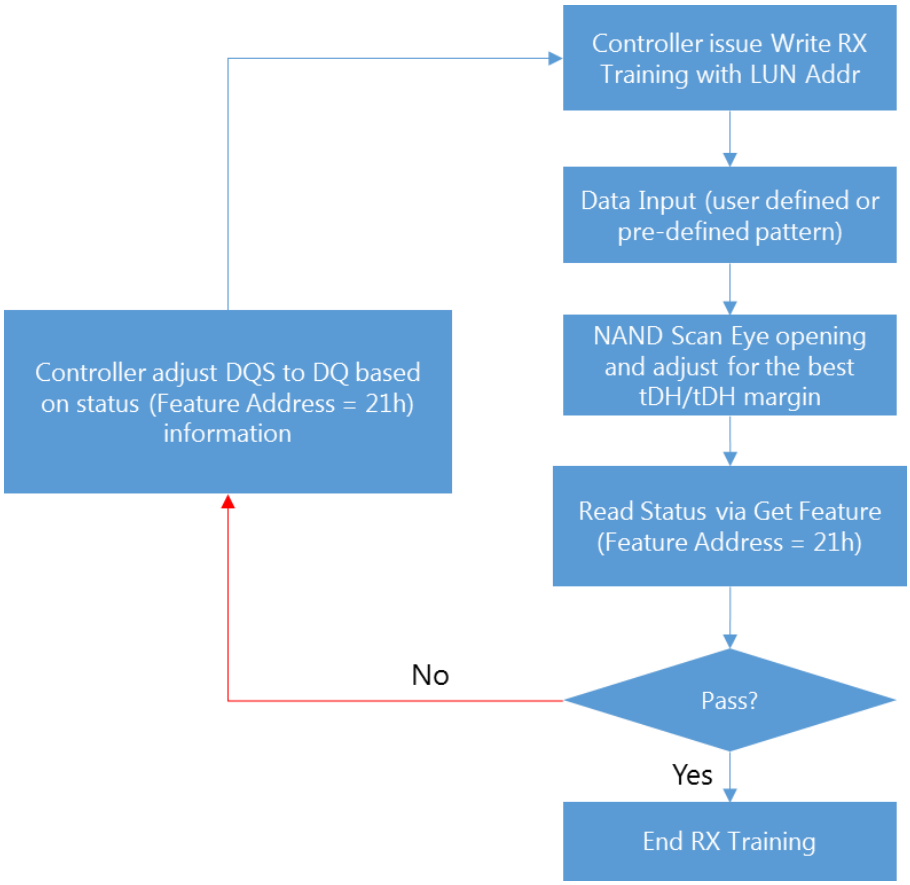


Figure 7-10 Flow chart for Write DQ Training (Rx side)

7.10. DQS Oscillator

As voltage and temperature change on the NAND die, the DQS clock tree delay will shift and may require re-training. NAND devices may include an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen later. The DQS oscillator count value reported by NAND device can be used by the memory controller to periodically train DQS to the DQ data valid window.

The DQS Oscillator is initiated using command 0Bh followed by LUN address (00h for single LUN, 01h for All LUN). Host shall wait time (tOSCready) such that NAND internal DQS oscillator is ready, and host cannot issue any command on the same CE during tOSCready. The DQS oscillator can be started by issuing 00h address cycle, which will start an internal oscillator that counts the number of times a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator can be stopped by issuing 00h address cycle. When the DQS oscillator is stopped, the results of the oscillator counter is automatically stored in P1[7:0] and P2[7:0] of FA26h and host can read these values using get feature (FA26h). P1[7:0] contains the least significant bits (LSBs) of the result. P2[7:0] contains the most significant bits (MSBs) of the result. And next CMD can be issued after waiting oscillator completion time (tOSCPOST). If a user issues any command other than 'Get Feature or Get Feature by LUN' right after tOSCPOST, the previous DQS oscillator counter result will be invalid because the voltage and temperature environment can be different between DQS oscillator and other operations.

During the DQS oscillator internal operation from start to stop address cycles, an interleaving operation except for FFh on the same CE_n/CA_CE_n is not allowed.

When user wants to perform DQS oscillator, the user shall keep CE# 'Low' during DQS oscillator operation. If a NAND enters a low power standby state while DQS oscillator is operating, a NAND will stop operating the oscillator and the counter results stored in FA26h P1[7:0] and P2[7:0] are invalid and shall be ignored.

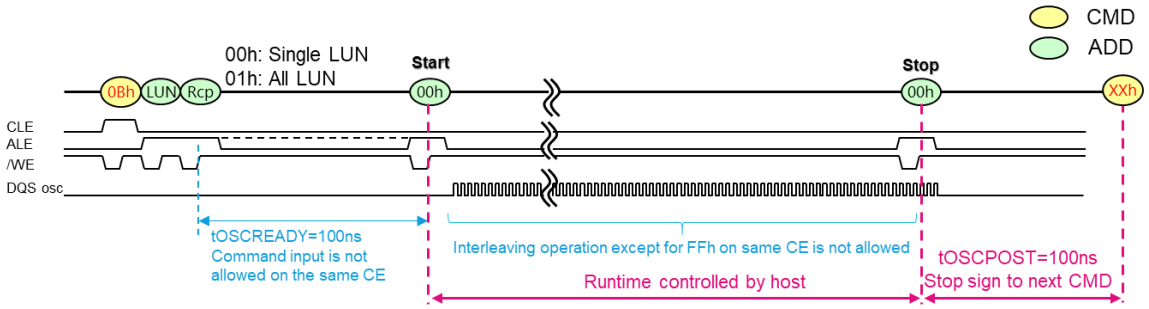


Figure 7-11 Conv. Protocol DQS Oscillator Operation Sequence and Timing

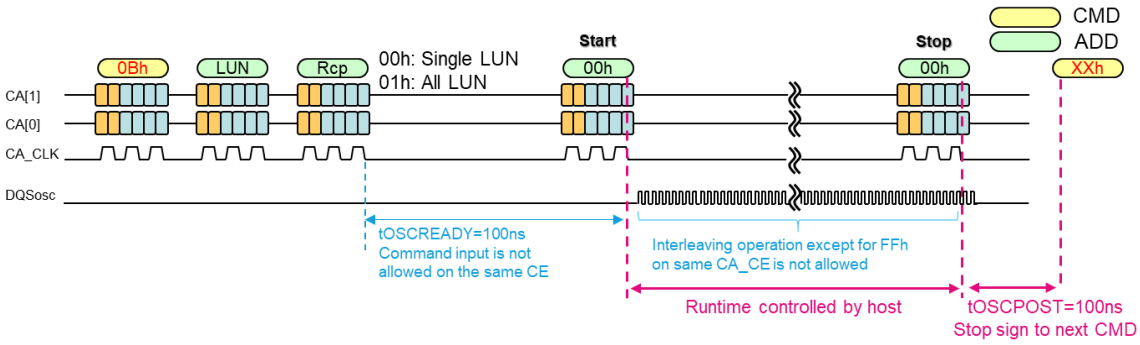


Figure 7-12 SCA Protocol DQS Oscillator Operation Sequence and Timing

CMD	1st Address cycle	2nd Address cycle	DQS Oscillator Operation
0Bh	LUN address (XXh)	00h	Operation in the selected single LUN
0Bh	00h	01h	Operation in all LUN

Table 7-1 DQS Oscillator Operation Modes Versus 2nd Address Cycle

Parameter	Symbol	Min	Max	Unit
Minimum time controller needs to provide during DQS Osc sequence, between Single LUN/All LUN address cycle to the 00h Start address cycle	$tOSC_{ready}$	100	-	ns

Table 7-2 tOSCready Specification

The controller may adjust the accuracy of the result by running the DQS Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

- DQS oscillator granularity error = 2*tDQS2DQ / Runtime

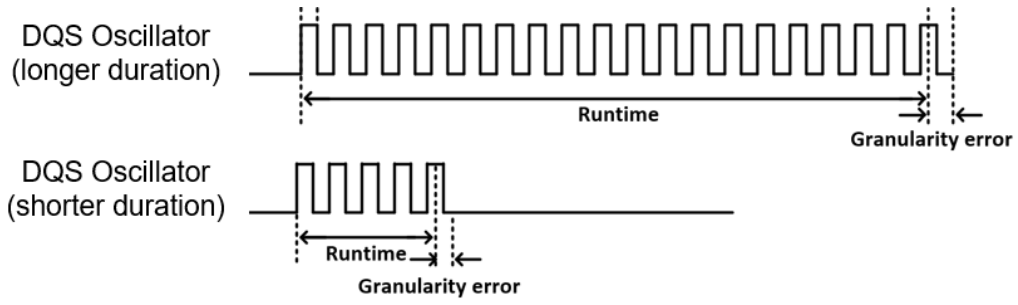


Figure 7-13 DQS Oscillator Granularity Error

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. Therefore, the total accuracy of the DQS oscillator counter is given by the following equation:

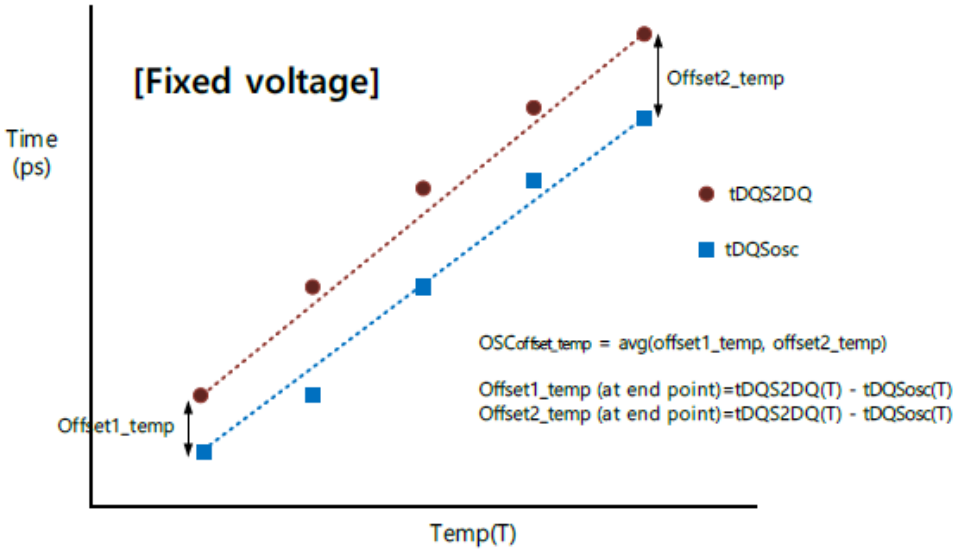
DQS Oscillator accuracy = 1 – Granularity Error – Matching Error

The NAND flash DQS oscillator counter will count to its maximum value(=216-1= FFFFh) and stop. The longest runtime for the oscillator that will not overflow the counter registers can be calculated as follows:

Longest tDQS2DQ runtime interval = 216 * [2*tDQS2DQ(min)] = 216 * [2*100ps] = 13.1072 μ s
Users should set DQS oscillator runtime below longest tDQS2DQ runtime interval for the counter code not to be overflowed.

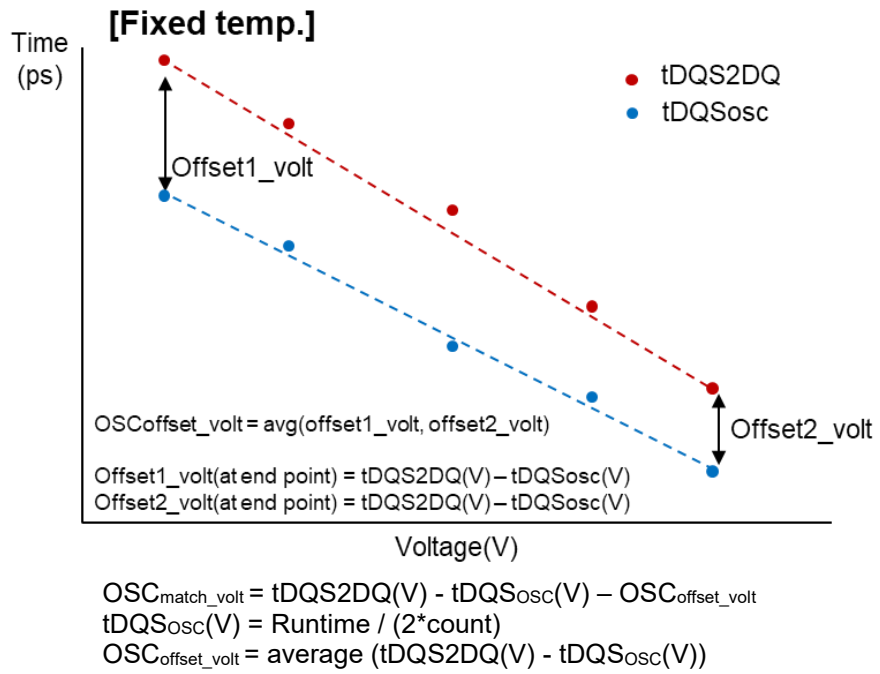
7.10.1. DQS Oscillator Matching Error

The DQS Oscillator matching error is defined as the difference between the DQS Oscillator circuit ($tDQS_{OSC}$) and the actual DQS clock tree (tDQS2DQ) across voltage and temperature.



OSC_{match_temp} = tDQS2DQ(T) - $tDQS_{OSC}$(T) – OSC_{offset_temp}
$tDQS_{OSC}$(T) = Runtime / (2*count)
OSC_{offset_temp} = average (tDQS2DQ(T) - $tDQS_{OSC}$(T))

Figure 7-14 DQS Oscillator offset_temp



OSC_{match_volt} = tDQS2DQ(V) - $tDQS_{OSC}$(V) – OSC_{offset_volt}
$tDQS_{OSC}$(V) = Runtime / (2*count)
OSC_{offset_volt} = average (tDQS2DQ(V) - $tDQS_{OSC}$(V))

Figure 7-15 DQS Oscillator offset_volt

Parameter	Symbol	Min	Max	Unit	Notes
DQS Oscillator Matching Error: voltage variation	OSC_{match_volt}	-25	25	ps	1, 2
DQS Oscillator Matching Error: temperature variation	OSC_{match_temp}	-25	25	ps	1, 2
DQS Oscillator Offset for voltage variation	OSC_{offset_volt}	-200	200	ps	2
DQS Oscillator Offset for temperature variation	OSC_{offset_temp}	-200	200	ps	2

Note1: The OSC_{match} is the matching error between the actual DQS and DQS oscillator over voltage and temp.
Note2: This parameter will be characterized or guaranteed by design.

Figure 7-16 DQS Oscillator Matching Error Specifications

7.11. Write Training Monitor (Optional)

Write Training Monitor is a method by which systems can monitor the effects of voltage and temperature changes on system timing margins. With voltage and temperature changes on the system, there is a need for a method to monitor whether the last obtained optimum training

settings are still sufficient to produce low error rates on the interface. A method to monitor sufficiency of the last obtained optimum settings is described below:

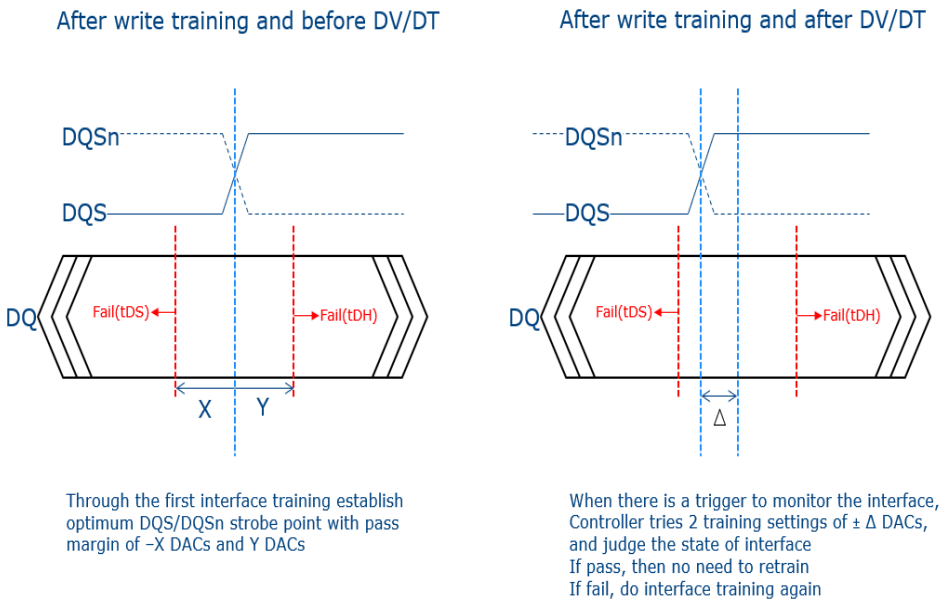


Figure 7-17 Write Training Monitoring Method

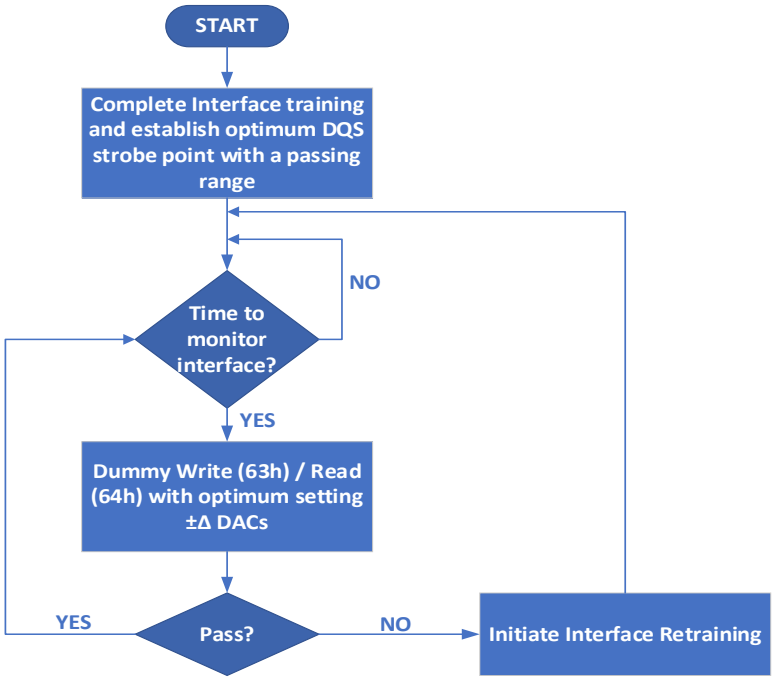


Figure 7-18 Write Training Monitor Flowchart

8. Feature Parameter Definitions

NAND devices only support feature parameters defined in ONFI specification revisions that they comply with.

Feature settings are volatile across power cycles. For each feature setting, whether the value across resets is retained is explicitly stated.

Reserved bits shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

Feature Address	Description
00h	Reserved
01h	Timing Mode
02h	Interface Configuration
03h-0Fh	Reserved
10h	I/O Pull-Down Drive Strength
11h-1Fh	Reserved
20h	DCC, Read, Write Tx Training
21h	Write Training RX
22h	Channel ODT, SCA Non-Target ODT Configuration
23h	Internal VrefQ value
24h	Write Duty Cycle Adjustment (WDCA)
25h	Reserved
26h	DQS Oscillator
27h	Decision Feedback Equalizer (DFE)
28h	Read Duty Cycle Adjustment (RDCA)
29h-2Fh	Reserved
30h	External Vpp Configuration
31h-3Fh	Reserved
40h	Per-Pin Vrefq Training
41h	Per-Pin Vrefq Training
42h	Reserved
43h-4Fh	Reserved
50h	Reserved
51h-57h	Reserved
58h	Volume Configuration
59h-5Fh	Reserved
60h	Reserved
61h	Reserved
62h-7Fh	Vendor specific
80h-FFh	Vendor specific

Table 8-1 Feature Parameter Addresses

8.1. FA 01h: Program Clear

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	R	PC[1]	Reserved (0)					
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							
Note: 1. Vendor Specific								

Table 8-2 Feature Address 01h

PC — The Program Clear bit controls the program page register clear enhancement which defines the behavior of clearing the page register when a Program (80h) command is received. If cleared to zero, then the page register(s) for each LUN that is part of the target is cleared when the Program (80h) command is received. If set to one, then only the page register for the LUN and interleave address selected with the Program (80h) command is cleared and the tADL time for Program commands is as reported in the parameter page. This bit is vendor specific. Please see vendor datasheet for support of the program clear feature

8.2. FA 02h: Interface Configuration Register

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

It is recommended to configure this register while in Timing Mode 0. The host shall take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	ODT Self-Termination				R	CMPR	CMPD	R
P2	Warmup DQS cycles for Data Input				Warmup RE_n and DQS cycles for Data Output			
P3	VSP	VOH.LTT	DBI.WR	DBI.RD	Internal VREFQ Range	Interface Type		
P4	Reserved (R)						SCA_DQMIRR	SCA_OUT

Table 8-3 Feature Address 02h

CMPD — If set to one, then the complementary DQS (DQS_c) signal is enabled. If cleared to zero, then the complementary DQS (DQS_c) signal is not used. The default value of this field is vendor specific, please see vendor datasheet.

CMPR

If set to one, then the complementary RE_n (RE_c) signal is enabled. If cleared to zero, then the complementary RE_n (RE_c) signal is not used. The default value of this field is vendor specific, please see vendor datasheet.

ODT Self-Termination

This field controls the on-die termination settings for the DQ[7:0], DBI, DQS_t, DQS_c, RE_t, and RE_c signals. The values are:

0h = ODT disabled
1h = ODT enabled with Rtt of 150 Ohms
2h = ODT enabled with Rtt of 100 Ohms (Optional)
3h = ODT enabled with Rtt of 75 Ohms
4h = ODT enabled with Rtt of 50 Ohms
5h = ODT enabled with Rtt of 30 Ohms (Optional)

Note: Rtt settings may be specified separately for DQ[7:0]/DQS and the RE_n signals. The DQ[7:0]/DQS/DBI may be specified separately for data input versus data output operation. Refer to the definition of the ODT Configure command in section 6.25. If values are specified with the ODT Configure command, then this field is not used. Get Features returns the previous value set in this field, regardless of the Rtt settings specified using ODT Configure.

Warmup RE_n and DQS cycles for Data Output

This field indicates the number of warmup cycles of RE_n and DQS that are provided for data output. These are the number of initial “dummy” RE_t/RE_c cycles at the start of data output operations. There are corresponding “dummy” DQS_t/DQS_c cycles to the “dummy” RE_t/RE_c cycles that the host shall ignore. The values are:

0h = 0 cycles, feature disabled
1h = 1 warmup cycle
2h = 2 warmup cycles
3h = 4 warmup cycles
4h-FFh = Reserved

Warmup DQS cycles for Data Input

This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial “dummy” DQS_t/DQS_c cycles at the start of data input operations. The values are:

0h = 0 cycles, feature disabled
1h = 1 warmup cycle
2h = 2 warmup cycles
3h = 4 warmup cycles
4h-FFh = Reserved

Interface Type (optional)

This field may be used to optionally enable NV-LPDDR4 with VccQL (PI-LTT)

0h = Reserved
1h = NV-LPDDR4 (LTT) (default)
2h = NV-LPDDR4 with VccQL (PI-LTT)

3h = Reserved

Internal VrefQ Range (Read Only)

This field indicates the range and step size of the internal VrefQ settings

0h = Range/Step Size Type 1/Value 1
1h = Range/Step Size Type 2/Value 2
2h = Range/Step Size Type 3/Value 3
3h = Reserved

DBI.RD (optional)

This field controlls the DBI usage for Read data transfers. If set to 1 then DBI is enabled, if cleared to 0 then DBI is disabled for Read data transfers.

DBI.WR (optional)

This field controlls the DBI usage for Write data transfers. If set to 1 then DBI is enabled, if cleared to 0 then DBI is disabled for Write data transfers.

VOH.LTT (optional)

This field may optionally be supported. When set to 1 then VOH.LTT nominal is VccQ/2.5, if cleared to 0 then VOH.LTT nominal is VccQ/3.

SCA_OUT (optional, SCA)

This field controls the SCA protocol CA output packet format

0h (default) = single-byte CA output format
1h = multi-byte CA output format

SCA_DQMIRR (optional, SCA)

This field controls SCA protocol DQ mirror function enable/disable

0h (default) = DQ mirror function disabled
1h = DQ mirror function enabled

8.3. FA 10h: I/O Pull-Down Drive Strength

For the NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces, FA10h P1[3:0] controls the drive strength of the pull-down device while the output drive strength of the pull-up device is controlled by FA22h P1[3:0] Channel ODT settings.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)				PDN Drive Strength			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-4 Feature Address 10h

Drive strength
0000b: 18 Ohm (Optional)
0001b: 25 Ohm (Optional)
0010b: 37.5 Ohm
0011b: 50 Ohm
0100b: 37.5 Ohm (power-on default)

8.4. FA 20h: DCC Training, Read Training, Write Training Tx

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)					DCC Factory setting	DCCI_EN	DCCE_EN
P2	Reserved (0)							
P3	Reserved (0)			Read training defined pattern length	Write Training Tx Data Size			
P4	Reserved (0)							

Table 8-5 Feature Address 20h

DCCE_EN

This field controls explicit DCC training setting. If set to 1 then DCC training is enabled, if cleared to 0 then DCC training is disabled.

DCCI_EN

This field controls implicit DCC training during warm up cycles setting. If set to 1 then DCC training is enabled, if cleared to 0 then DCC training is disabled. A host can disable DCCI_EN if the host doesn't need DCC with low frequency operation.

DCC Factory setting

This is an optional function for the NAND device, please refer to the vendor datasheet if DCC factory setting is supported or not. If set to a 1, then the factory DCC settings would be used by the LUN. If cleared to 0, then the DCC calibrated settings would be used by the LUN.

Write Training Tx Data Size (Read Only)

This field indicates the data size for write training (Tx side) (up to 128bytes). NAND devices may support a Write Training (Tx side)

data size less than or greater than the value specified on these bits. See vendor data sheet for details on the vendor implementation of these bits.

0000b: 08 Bytes
0001b: 16 Bytes
0010b: 24 Bytes
0011b: 32 Bytes
0100b: 40 Bytes
0101b: 48 Bytes
0110b: 56 Bytes
0111b: 64 Bytes
1000b: 72 Bytes
1001b: 80 Bytes
1010b: 88 Bytes
1011b: 96 Bytes
1100b: 104 Bytes
1101b: 112 Bytes
1110b: 120 Bytes
1111b: 128 Bytes

Read Training Defined pattern length (Read Only)

This field indicates the data pattern length for read training
1b: 32 Bytes
0b: 16 Bytes

8.5. FA 21h: Write Training Rx

The following Sub Feature parameters are to be used for Write Training (Rx side):

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)					Internal VrefQ Training	All LUN	Factory setting
P2	St_dq3[1:0]		St_dq2[1:0]		St_dq1[1:0]		St_dq0[1:0]	
P3	St_dq7[1:0]		St_dq6[1:0]		St_dq5[1:0]		St_dq4[1:0]	
P4	Reserved (0)							

Table 8-6 Feature Address 21h

Factory setting

This field controls the input path settings as determined by training/reset or factory settings.
1b: factory setting
0b: trained value

All LUN

This is an optional function for the NAND device, please refer to the vendor datasheet if All LUN Write Training (Rx side) is supported or not. If this bit is set to 1 prior to write training RX, then the LUN address cycle is ignored, and the write training is performed on all LUNs.

Internal VrefQ Training

This is an optional function for the NAND device, please refer to the vendor datasheet if internal Vrefq Training during Write Training (Rx side) is supported or not. Setting this bit to 1 enables Write Training (Rx side) with internal VrefQ Training. Clearing the bit to 0 enables normal Write Training (Rx side).

St_dq (Read Only)

These fields indicate the status of the Rx side Write Training (DQ[3:0] in sub parameter P2, DQ[7:4] in sub parameter P3).
00b: Centering of dqs to dq0 data eye is successful.
01b: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too slow with respect to dqs/dqsn
10b: Centering of dqs/dqsn to dq0 data eye failed with dq0 being too fast with respect to dqs/dqsn
11b: Centering of dqs/dqsn to dq0 data eye failed for unknown reasons

8.6. FA 22h: Channel ODT, SCA Non-Target ODT Configuration

The channel ODT (CH_ODT) setting controls the strength of the output pull-up device on the NAND. Using the channel ODT setting the host tells the NAND the ODT strength on the channel during NAND data output operations and the NAND adjusts the strength of its output pull-up devices accordingly to support the VOH,nom value. The channel ODT setting values that are supported are vendor specific. commands. The power-on default channel ODT value is 50 Ohm (0110b).

The SCA_NTODT_DIN, SCA_NTODT_RE and SCA_NTODT_DOUT bits are the non-target ODT settings for a LUN when SCA is enabled.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh).

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	Reserved (0)				Channel ODT (CH_ODT)			
P2	Reserved (0)				SCA Non-Target ODT for DQ/DQS/DBI during Data Input (SCA_NTODT_DIN)			
P3	Reserved (0)				SCA Non-Target ODT for RE during Data Output (SCA_NTODT_RE)			
P4	Reserved (0)				SCA Non-Target ODT for DQ/DQS/DBI during Data Output (SCA_NTODT_DOUT)			

Table 8-7 Feature Address 22h

Channel ODT setting
0000b-0001b: Reserved
0010b: 150 Ohms
0011b: 100 Ohms
0100b: 75 Ohms
0101b: 60 Ohms

0110b: 50 Ohms (default)
0111b: 37.5 Ohms
1000b: 25 Ohms
1001b-1111b Reserved

SCA_NTODT_DIN/
SCA_NTODT_RE/
SCA_NTODT_DOUT setting
0h = Non-Target ODT disabled
1h = Non-Target ODT enabled with Rtt of 150 Ohms
2h = Non-Target ODT enabled with Rtt of 100 Ohms (Optional)
3h = Non-Target ODT enabled with Rtt of 75 Ohms
4h = Non-Target ODT enabled with Rtt of 50 Ohms
5h = Non-Target ODT enabled with Rtt of 30 Ohms (Optional)
6h-Fh = Reserved

8.7. FA 23h: Internal VrefQ Value

This feature register provides the ability to control the internal VrefQ of a LUN for both NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) interfaces.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

The power-on default internal VrefQ value is 35% of VccQ or VccQL setting (46h).

The NAND internal VrefQ shall not be set to a setting beyond the allowable range even during Write Training. NAND is not required to implement VrefQ beyond the NAND Minimum Internal VrefQ Allowable Range.

Sub Feature Parameter	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P1	Internal VrefQ Value1/Value2/Value3 settings							Reserved
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-8 Feature Address 23h

Internal VrefQ Value

This field controls the voltage level of the internal VrefQ.

Internal VrefQ Value1 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	35%			VccQ
Vref_min	0%	-	-	VccQ
Vref_max	-	-	63.50%	VccQ
Vref_step	0.35%	0.50%	0.65%	VccQ

Vref_Set_Tol	-1.75%	0%	1.75%	VccQ

Table 8-9 NV-LPDDR4 (LTT) Internal VrefQ Value Range/Step-Size/Tolerance for Type1 or Value1 Settings

Internal VrefQ Value1 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default		35%		VccQL
Vref_min	0%	-	-	VccQL
Vref_max	-	-	63.50%	VccQL
Vref_step	0.35%	0.50%	0.65%	VccQL
Vref_Set_Tol	-2.63%	0%	2.63%	VccQL

Table 8-10 NV-LPDDR4 with VccQL (PI-LTT) Internal VrefQ Value Range/Step-Size/Tolerance for Type1 or Value1 Settings

Internal VrefQ Code	VrefQ (% of VccQ or VccQL)	Internal VrefQ Code	VrefQ (% of VccQ or VccQL)	Internal VrefQ Code	VrefQ (% of VccQ or VccQL)	Internal VrefQ Code	VrefQ (% of VccQ or VccQL)
00h	0.00	20h	16.00	40h	32.00	60h	48.00
01h	0.50	21h	16.50	41h	32.50	61h	48.50
02h	1.00	22h	17.00	42h	33.00	62h	49.00
03h	1.50	23h	17.50	43h	33.50	63h	49.50
04h	2.00	24h	18.00	44h	34.00	64h	50.00
05h	2.50	25h	18.50	45h	34.50	65h	50.50
06h	3.00	26h	19.00	46h	35.00	66h	51.00
07h	3.50	27h	19.50	47h	35.50	67h	51.50
08h	4.00	28h	20.00	48h	36.00	68h	52.00
09h	4.50	29h	20.50	49h	36.50	69h	52.50
0Ah	5.00	2Ah	21.00	4Ah	37.00	6Ah	53.00
0Bh	5.50	2Bh	21.50	4Bh	37.50	6Bh	53.50
0Ch	6.00	2Ch	22.00	4Ch	38.00	6Ch	54.00
0Dh	6.50	2Dh	22.50	4Dh	38.50	6Dh	54.50
0Eh	7.00	2Eh	23.00	4Eh	39.00	6Eh	55.00
0Fh	7.50	2Fh	23.50	4Fh	39.50	6Fh	55.50
10h	8.00	30h	24.00	50h	40.00	70h	56.00
11h	8.50	31h	24.50	51h	40.50	71h	56.50
12h	9.00	32h	25.00	52h	41.00	72h	57.00

13h	9.50	33h	25.50	53h	41.50	73h	57.50
14h	10.00	34h	26.00	54h	42.00	74h	58.00
15h	10.50	35h	26.50	55h	42.50	75h	58.50
16h	11.00	36h	27.00	56h	43.00	76h	59.00
17h	11.50	37h	27.50	57h	43.50	77h	59.50
18h	12.00	38h	28.00	58h	44.00	78h	60.00
19h	12.50	39h	28.50	59h	44.50	79h	60.50
1Ah	13.00	3Ah	29.00	5Ah	45.00	7Ah	61.00
1Bh	13.50	3Bh	29.50	5Bh	45.50	7Bh	61.50
1Ch	14.00	3Ch	30.00	5Ch	46.00	7Ch	62.00
1Dh	14.50	3Dh	30.50	5Dh	46.50	7Dh	62.50
1Eh	15.00	3Eh	31.00	5Eh	47.00	7Eh	63.00
1Fh	15.50	3Fh	31.50	5Fh	47.50	7Fh	63.50

Table 8-11 Internal VrefQ Value1 Setting Versus Value as % of VccQ or VccQL

For NAND devices that support Type2/Value2 settings (Vendor Specific, See Vendor datasheet) the following tables apply:

Internal VrefQ Value2 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	TBD			VccQ
Vref_min	0%	-	-	VccQ
Vref_max	-	-	99.22%	VccQ
Vref_step	0.58%	0.78%	0.98%	VccQ
Vref_Set_Tol	-1.95%	0%	1.95%	VccQ

Table 8-12 NV-LPDDR4 (LTT) Internal VrefQ Value Range/Step-Size/Tolerance for Type2 or Value2 Settings

Internal VrefQ Value2 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	TBD			VccQL
Vref_min	0%	-	-	VccQL
Vref_max	-	-	99.22%	VccQL
Vref_step	0.58%	0.78%	0.98%	VccQL
Vref_Set_Tol	-2.93%	0%	2.93%	VccQL

Table 8-13 NV-LPDDR4 with VccQL (PI-LTT) Internal VrefQ Value Range/Step-Size/Tolerance for Type2 or Value2 Settings

Internal VrefQ Code	VrefQ (% of VccQ or VccQL)	Internal VrefQ Code	VrefQ (% of VccQ or VccQL)	Internal VrefQ Code	VrefQ (% of VccQ or VccQL)	Internal VrefQ Code	VrefQ (% of VccQ or VccQL)
00h	0.00	20h	25.00	40h	50.00	60h	75.00
01h	0.78	21h	25.78	41h	50.78	61h	75.78
02h	1.56	22h	26.56	42h	51.56	62h	76.56
03h	2.34	23h	27.34	43h	52.34	63h	77.34
04h	3.13	24h	28.13	44h	53.13	64h	78.13
05h	3.91	25h	28.91	45h	53.91	65h	78.91
06h	4.69	26h	29.69	46h	54.69	66h	79.69
07h	5.47	27h	30.47	47h	55.47	67h	80.47
08h	6.25	28h	31.25	48h	56.25	68h	81.25
09h	7.03	29h	32.03	49h	57.03	69h	82.03
0Ah	7.81	2Ah	32.81	4Ah	57.81	6Ah	82.81
0Bh	8.59	2Bh	33.59	4Bh	58.59	6Bh	83.59
0Ch	9.38	2Ch	34.38	4Ch	59.38	6Ch	84.38
0Dh	10.16	2Dh	35.16	4Dh	60.16	6Dh	85.16
0Eh	10.94	2Eh	35.94	4Eh	60.94	6Eh	85.94
0Fh	11.72	2Fh	36.72	4Fh	61.72	6Fh	86.72
10h	12.50	30h	37.50	50h	62.50	70h	87.50
11h	13.28	31h	38.28	51h	63.28	71h	88.28
12h	14.06	32h	39.06	52h	64.06	72h	89.06
13h	14.84	33h	39.84	53h	64.84	73h	89.84
14h	15.63	34h	40.63	54h	65.63	74h	90.63
15h	16.41	35h	41.41	55h	66.41	75h	91.41
16h	17.19	36h	42.19	56h	67.19	76h	92.19
17h	17.97	37h	42.97	57h	67.97	77h	92.97
18h	18.75	38h	43.75	58h	68.75	78h	93.75
19h	19.53	39h	44.53	59h	69.53	79h	94.53
1Ah	20.31	3Ah	45.31	5Ah	70.31	7Ah	95.31
1Bh	21.09	3Bh	46.09	5Bh	71.09	7Bh	96.09
1Ch	21.88	3Ch	46.88	5Ch	71.88	7Ch	96.88
1Dh	22.66	3Dh	47.66	5Dh	72.66	7Dh	97.66
1Eh	23.44	3Eh	48.44	5Eh	73.44	7Eh	98.44
1Fh	24.22	3Fh	49.22	5Fh	74.22	7Fh	99.22

Table 8-14 Internal VrefQ Value2 Setting Versus Value as % of VccQ or VccQL

Notes:

1) The NAND internal VrefQ shall not be set to a setting beyond the allowable range even during Write Training.

2) NAND is not required to implement VrefQ beyond the NAND Minimum Internal VrefQ Allowable Range.

For NAND devices that support Type3/Value3 settings (Vendor Specific, See Vendor datasheet) the tables below apply:

Internal VrefQ Type3 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	Vendor Specific			VccQ
Vref_min	Vendor Specific			VccQ
Vref_max	Vendor Specific but has to be greater than NAND Minimum Internal VrefQ Allowable max values			VccQ
Vref_step	Vendor specific. Vendor can specify Vref_step Typ to be within 0.25% - 0.75% of VccQ			VccQ
Vref_Set_Tol	-1.75%	0%	1.75%	VccQ

Table 8-15 NV-LPDDR4 (LTT) Internal Vrefq Value Range/Step-Size for Type3 or Value3 settings

Internal VrefQ Type3 Range/Step Size				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Default	Vendor Specific			VccQL
Vref_min	Vendor Specific			VccQL
Vref_max	Vendor Specific but has to be greater than NAND Minimum Internal VrefQ Allowable max values			VccQL
Vref_step	Vendor specific. Vendor can specify Vref_step Typ to be within 0.25% - 0.75% of VccQ			VccQL
Vref_Set_Tol	-2.63%	0%	2.63%	VccQL

Table 8-16 NV-LPDDR4 with VccQL (PI-LTT) Internal Vrefq Value Range/Step-Size for Type3 or Value3 settings

For NAND devices that support Value3 settings:

- VREFI is the VrefQ voltage inside the NAND. VREFI is calculated in the following manner: VREFI = (VrefQ Setting)*Vref_step + Vref_min.
- VrefQ Setting can range from 0 ~ 255 (8b)
- If the calculated VREFI ≥ Vref_max, then actual VREFI = Vref_max
- A table showing feature address register setting versus the expected actual VREFI value can be derived using the formula above and represented in the vendor datasheet.

8.8. FA 24h: Write Duty Cycle Adjustment (WDCA)

This register contains bits that control the Write Duty Cycle Adjustment (WDCA) feature.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1				WDCA Step Control				
P2	Reserved							
P3	Reserved							
P4	Reserved							

Table 8-17 Feature Address 24h, WDCA

P1[4:0] for WDCA Step Control
- 00000b: 0step (default)
- 00001b: +1step
- 00010b: +2steps
- 00011b: +3steps
- 00100b ~ 01111b: +4steps ~ +15steps (Optional)
- 10000b: 0step
- 10001b: -1step
- 10001b: -2steps
- 10011b: -3steps
- 10100b ~ 11111b: -4steps ~ -15steps (Optional)

8.9. FA 26h: DQS Oscillator

This register contains bits related to the DQS Oscillator feature.

After performing the DQS Oscillator sequence and waiting tOSCPOST delay, the P2[7:0] DQS Oscillator Count – MSB field contains the MSB of the DQS oscillator count while the P1[7:0] DQS Oscillator Count – LSB field contains the LSB of the count.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	DQS Oscillator Count – LSB (Read Only)							
P2	DQS Oscillator Count – MSB (Read Only)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-18 Feature Address 26h, DQS Oscillator

8.10. FA 27h: Decision Feedback Equalizer (DFE)

This register contains bits related to the Decision Feedback Equalizer (DFE) feature.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Pre-drive for Read		Pre-drive for Write		R	DFE Coefficient Control		
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-19 Feature Address 27h, DFE

P1[2:0] for DFE Coefficient Control
- 000b (default) = disabled
- 001b = +1 step
- 010b = +2 steps
- 011b = +3 steps
- 100b = +4 steps (optional)
- 101b = +5 steps (optional)
- 110b = +6 steps (optional)
- 111b = +7 steps (optional)

P1[5:4] for Pre-drive for Write (NAND DFE)
- 00b (default) = disabled
- 01b = Pre-drive 2UI
- 10b = Pre-drive 4UI (optional)
- 11b = Pre-drive 8UI (optional)

P1[7:6] for Pre-drive for Read (Controller DFE)
- 00b (default) = disabled
- 01b = Pre-drive 2UI
- 10b = Pre-drive 4UI (optional)
- 11b = Pre-drive 8UI (optional)

8.11. FA 28h: Read Duty Cycle Adjustment (RDCA)

This register contains bits related to the Read Duty Cycle Adjustment (RDCA) feature.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)			RDCA Step Control				
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-20 Feature Address 28h, RDCA

P1[4:0] for RDCA Step Control
- 00000b: 0step (default)
- 00001b: +1step
- 00010b: +2steps
- 00011b: +3steps
- 00100b ~ 01111b: +4steps ~ +15steps (Optional)

10000b: 0step
10001b: -1step
10001b: -2steps
10011b: -3steps
10100b ~ 11111b: -4steps ~ -15steps (Optional)

8.12. FA 30h: External Vpp Configuration

This register shall be supported if the target supports external Vpp as specified in the parameter page. This setting controls whether external Vpp is enabled.

The settings in this register are retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands. The power-on default is 0h for all fields.

Vpp must be valid prior to the Set Feature that enables Vpp.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)							Vpp
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-21 Feature Address 30h, VPP COnfiguration

Vpp
0b = External Vpp is disabled
1b = External Vpp is enabled

8.13. FA 40h and FA 41h: Per-Pin VREFQ Offsets

This register contains bits related to the Per-Pin VREFQ Offsets feature.

The settings in these registers are retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Vrefq Offset for DQ1				Vrefq Offset for DQ0			
P2	Vrefq Offset for DQ3				Vrefq Offset for DQ2			
P3	Vrefq Offset for DQ5				Vrefq Offset for DQ4			
P4	Vrefq Offset for DQ7				Vrefq Offset for DQ6			

Table 8-22 Feature Address 40h, Per-Pin Vrefq Adjustment DQ0-DQ7

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)				Vrefq Offset for DBI			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Table 8-23 Feature Address 41h, Per-Pin Vrefq Adjustment DBI

For each Vrefq Offset setting in FA40h and FA41h:

0000b: 0 step offset (default)
0001b: +1 step offset
0010b: +2 steps offset
0011b: +3 steps offset
0100b – 0111b: +4 ~ +7 steps offset
1000b: 0 step offset
1001b: -1 step offset
1010b: -2 steps offset
1011b: -3 steps offset
1100b – 1111b: -4 ~ -7 steps offset

8.14. FA 58h: Volume Configuration (Conv. Protocol Only)

This setting is used in the Conv. Protocol to configure the Volume Address and shall be supported for NAND Targets that indicate support for Volume Addressing in the parameter page. After the Volume Address is appointed, the Volume is deselected until a Volume Select command is issued that selects the associated Volume.

The host shall only set this feature once per power cycle for each Volume. The address specified is then used in Select Volume commands for accessing this NAND Target.

Settings in this register are retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. There is no default power-on value.

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved				Volume Address			
P2	Reserved							
P3	Reserved							
P4	Reserved							

Table 8-24 Feature Address 58h, Volume Address configuration

Volume Address Specifies the Volume address to appoint.

9. Multi-plane Operations

A LUN may support multi-plane read, program and erase operations. Multi-plane operations are when multiple commands of the same type are issued to different blocks on the same LUN. Refer to section 6.7.1.28 for addressing restrictions with multi-plane operations. There are two methods for multi-plane operations: concurrent and overlapped.

When performing multi-plane operations, the operations/functions shall be the same type. The functions that may be used in multi-plane operations are:

- Page Program
- Copyback Read and Program
- Block Erase
- Read

9.1. Requirements

When supported, the plane address comprises the lowest order bits of the block address as shown in Figure 3-3. The LUN address is required to be the same. The block address (other than the plane address bits) may be required to be the same, refer to section 6.7.1.28. Some devices or multi-plane operations may require page addresses to be the same as other multi-plane operations in the multi-plane command sequence. Refer to the vendor datasheet for the multi-plane operation restrictions applicable to the device.

For Copyback program operations, the restrictions are the same as for a multi-plane program operation. However, Copyback reads shall be previously issued to the same plane addresses as those in the multi-plane Copyback program operations. The reads for Copyback may be issued non-multi-plane or multi-plane. If the reads are non-multi-plane then the reads may have different page addresses. If the reads are multi-plane then the reads shall have the same page addresses.

Multi-plane operations enable operations of the same type to be issued to other blocks on the same LUN. There are two methods for multi-plane operations: concurrent and overlapped. The concurrent multi-plane operation waits until all command, address, and data are entered for all plane addresses before accessing the Flash array. The overlapped multi-plane operation begins its operation immediately after the command, address and data are entered and performs it in the background while the next multi-plane command, address, and data are entered.

The plane address component of each address shall be distinct. A single multi-plane (cached) program operation is shown in the figure below. Between “Multi-plane Op 1” and “Multi-plane Op n”, all plane addresses shall be different from each other. After the 10h or 15h (cached) command cycle is issued, previously issued plane addresses can be used in future multi-plane operations.

Figure 9-1 Multi-plane Program (Cache)

For multi-plane erase operations, the plane address component of each address shall be distinct. A single multi-plane erase operation is shown in the figure below. Between “Multi-plane Op 1” and “Multi-plane Op n”, all plane addresses shall be different from each other. After the D0h command cycle is issued, previously issued plane addresses can be used in future multi-plane operations.

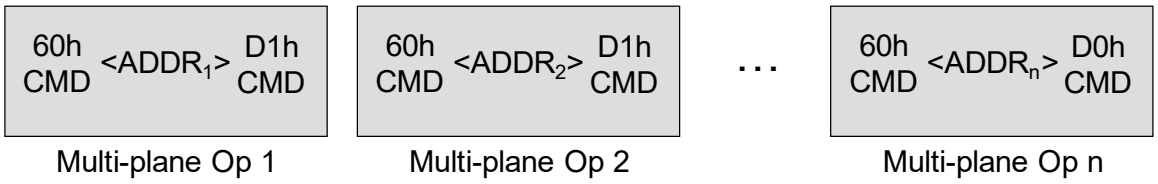


Figure 9-2 Multi-plane Erase

The plane address component of each address shall be distinct. A single multi-plane read (cache) operation is shown in the figure below. Between “Multi-plane Op 1” and “Multi-plane Op n”, all plane addresses shall be different from each other. After the 30h or 31h (cached) command cycle is issued, previously issued plane addresses can be used in future multi-plane operations.

Figure 9-3 Multi-plane Read (Cache)

9.2. Status Register Behavior

Some status register bits are independent per plane address. Other status register bits are shared across the entire LUN. This section defines when status register bits are independent per plane address. This is the same for concurrent and overlapped operations.

For multi-plane program and erase operations, the FAIL/FAILC bits are independent per plane address. The RDY and ARDY bits may be independent per plane address, see vendor datasheet. The table below lists whether a bit is independent per plane address or shared across the entire LUN for multi-plane operations.

Value	7	6	5	4	3	2	1	0
Status Register	WP_n	RDY	ARDY	VSP	VSP	VSP	FAILC	FAIL
Independent	N	VSP	VSP	N	N	N	Y	Y

Table 9-1 Independent Status Register bits

9.3. Multi-plane Page Program

The Page Program command transfers a page or portion of a page of data identified by a column address to the page register. The contents of the page register are then programmed into the Flash array at the row address indicated. With a multi-plane operation, multiple programs can be issued back-to-back to the LUN, with a shorter busy time between issuance of the next program operation. The figure below defines the behavior and timings for two multi-plane page program commands.

Cache operations may be used when doing multi-plane page program operations, as shown, if supported by the target as indicated in the parameter page. Refer to section 6.7.1.27.

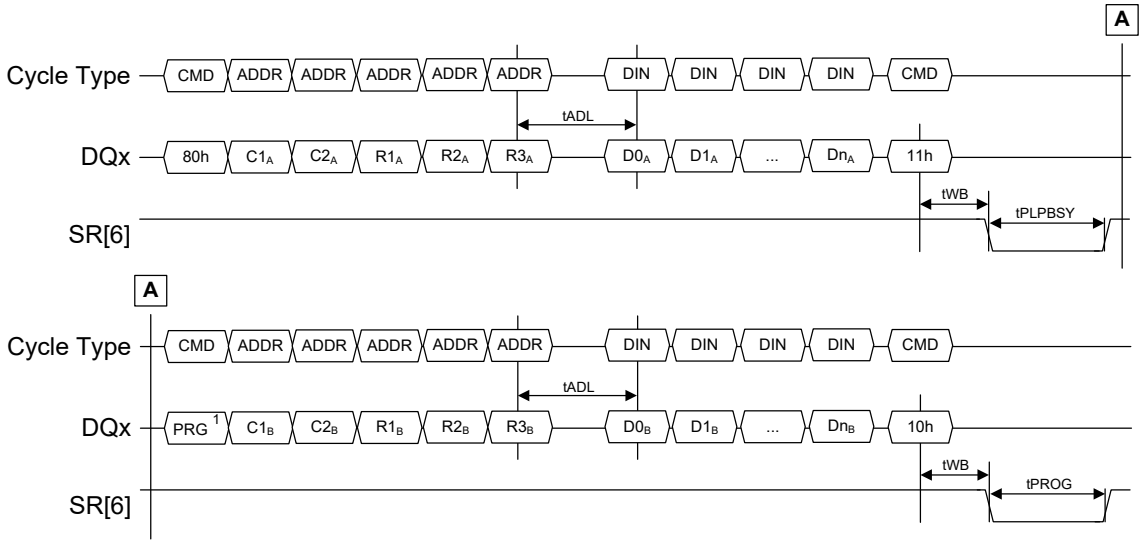


Figure 9-4 Multi-plane Page Program Timing

Notes:

1. There are two forms of Multi-plane Page Program. ONFI 1.x and 2.x revisions have defined all first cycles for all program sequences in a Multi-plane Page Program as 80h. The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial program sequence in a Multi-plane Page Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a program sequence as 81h.
2. NAND vendors may remove tPLPBSY busy time, keeping SR[6] HIGH between multi-plane sequences, and instead require the host to provide a vendor specific fixed delay between multi-plane sequences (see vendor datasheet).

$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.

$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.

$D0_A$-Dn_A Data to program for page A.

PRG 80h or 81h. Refer to Note 1.

$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.

$D0_B$-Dn_B Data to program for page B.

The row addresses for page A and B shall differ in the plane address bits.

Finishing a multi-plane program with a command cycle of 15h rather than 10h indicates that this is a cache operation. The host shall only issue a command cycle of 15h to complete a multi-plane program operation if program cache is supported with multi-plane program operations, as described in section 6.7.1.27.

9.4. Multi-plane Copyback Read and Program

The Copyback function reads a page of data from one location (via a Copyback Read) and then moves that data to a second location (via a Copyback Program). Copyback Read and Copyback Program may support multi-plane operations.

The figure below defines the behavior and timings for two Copyback non-multi-plane read sequences. The plane addresses used for the Copyback Read (regardless of non multi-plane or multi-plane) shall be the same as the plane addresses used in the subsequent multi-plane Copyback Program operations.

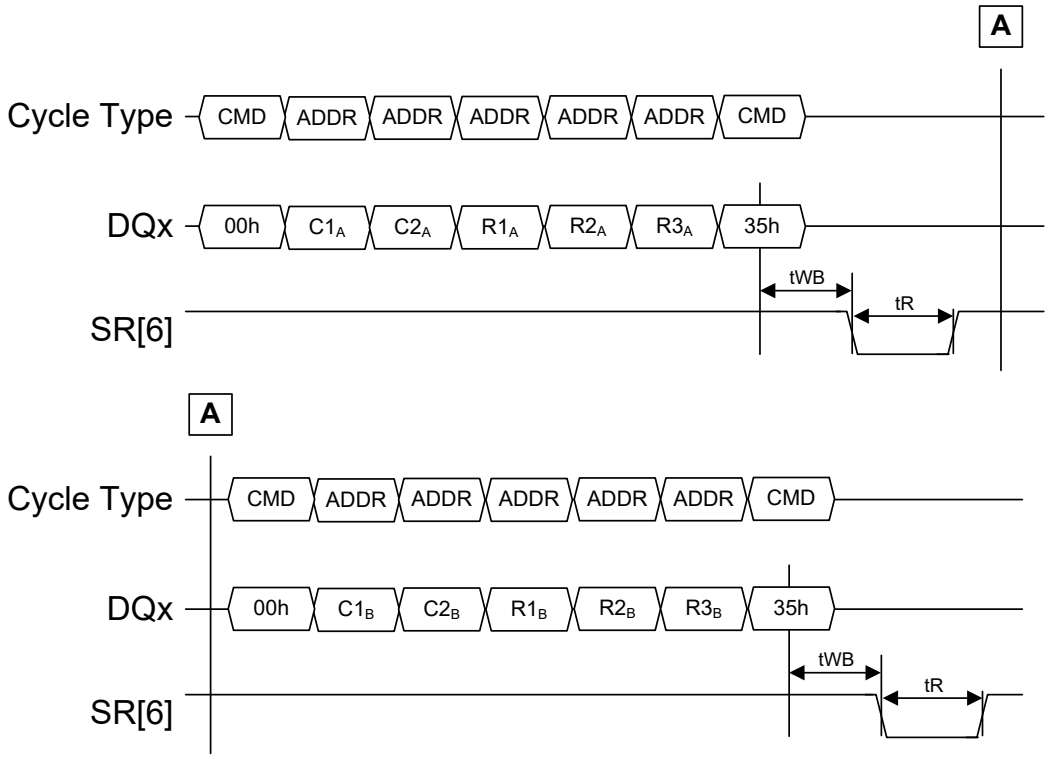


Figure 9-5 Non Multi-Plane Copyback Read Timing

$C1_A$-$C2_A$ Column address for source page A. $C1_A$ is the least significant byte.

$R1_A$-$R3_A$ Row address for source page A. $R1_A$ is the least significant byte.

$C1_B$-$C2_B$ Column address for source page B. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address for source page B. $R1_B$ is the least significant byte.

The row addresses for all source pages shall differ in their plane address bits.

The following figure defines the behavior and timings for a Multi-plane Copyback Read operation. The plane addresses used for the Copyback Read (regardless of non multi-plane or multi-plane) shall be the same as the plane addresses used in the subsequent multi-plane Copyback Program operations.

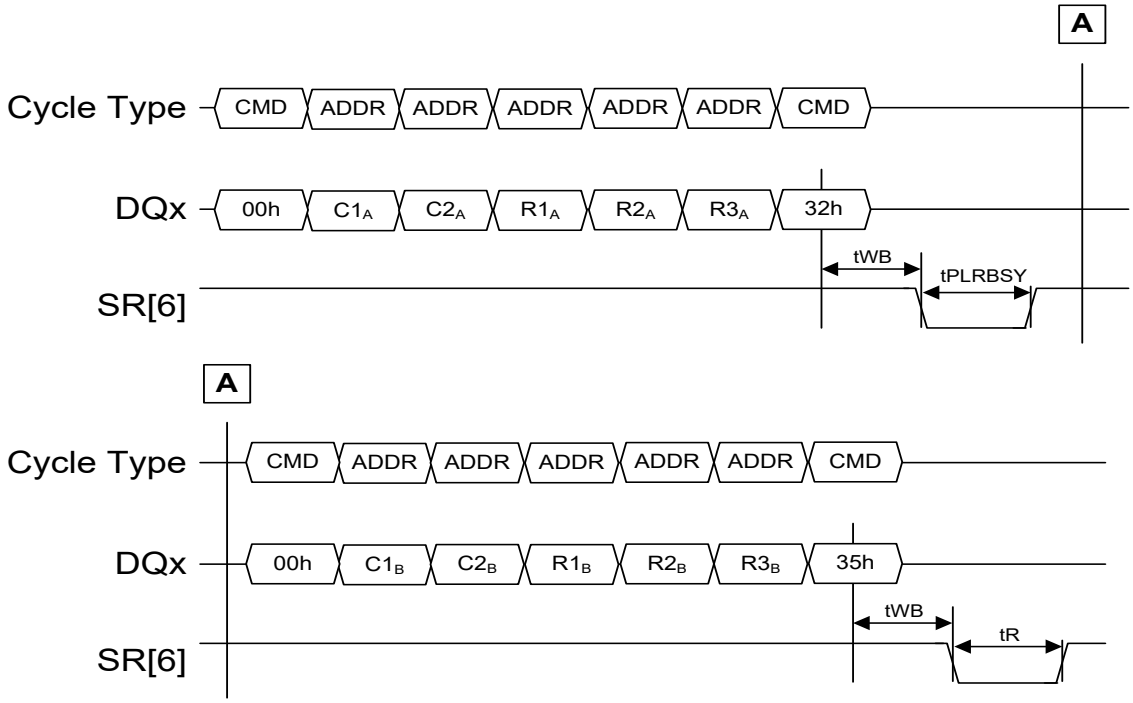


Figure 9-6 Multi-plane Copyback Read Timing

$C1_A$-$C2_A$	Column address for source page A. $C1_A$ is the least significant byte.
$R1_A$-$R3_A$	Row address for source page A. $R1_A$ is the least significant byte.
$C1_B$-$C2_B$	Column address for source page B. $C1_B$ is the least significant byte.
$R1_B$-$R3_B$	Row address for source page B. $R1_B$ is the least significant byte.

The row addresses for all source pages shall differ in their plane address bits. The source page addresses shall be the same for multi-plane reads.

The following figure defines the behavior and timings for a Multi-plane Copyback Program operation:

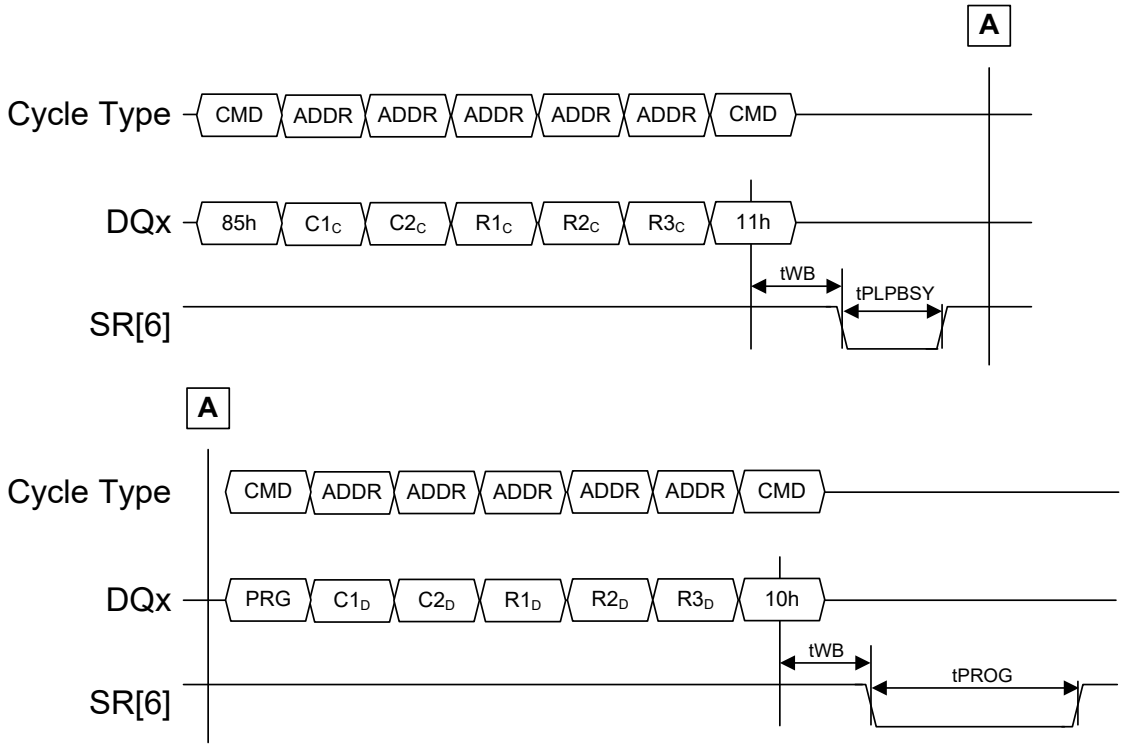


Figure 9-7 Multi-plane Copyback Program

Notes:

1. There are two forms of Multi-plane Copyback Program. ONFI 1.x and 2.x revisions have defined all first cycles for all program sequences in a Multi-plane Copyback Program as 85h. The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial Copyback Program sequence in a Multi-plane Copyback Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a Multi-plane Copyback Program sequence as 81h.
2. NAND vendors may remove tPLRBSY & tPLPBSY busy times, keeping SR[6] HIGH between multi-plane sequences, and instead require the host to provide a vendor specific fixed delay between multi-plane sequences (see vendor datasheet).

$C1_C$-$C2_C$ Column address for destination page C. $C1_C$ is the least significant byte.

$R1_C$-$R3_C$ Row address for destination page C. $R1_C$ is the least significant byte.

PRG 85h or 81h. Refer to Note 1.

$C1_D$-$C2_D$ Column address for destination page D. $C1_D$ is the least significant byte.

$R1_D$-$R3_D$ Row address for destination page D. $R1_D$ is the least significant byte.

The row addresses for all destination pages shall differ in their plane address bits. The page address for all destination addresses for multi-plane copyback operations shall be identical.

9.5. Multi-plane Block Erase

Figure 9-8 defines the behavior and timings for a multi-plane block erase operation. Only two operations are shown, however additional erase operations may be issued with a 60h/D1h sequence prior to the final 60h/D0h sequence depending on how many multi-plane operations the LUN supports.

The ONFI-JEDEC Joint Taskgroup has defined a modified version of multi-plane block erase, where subsequent row addresses specifying additional blocks to erase are not separated by D1h commands. This definition is shown in Figure 9-9. Refer to the parameter page to determine if the device supports not including the D1h command between block addresses.

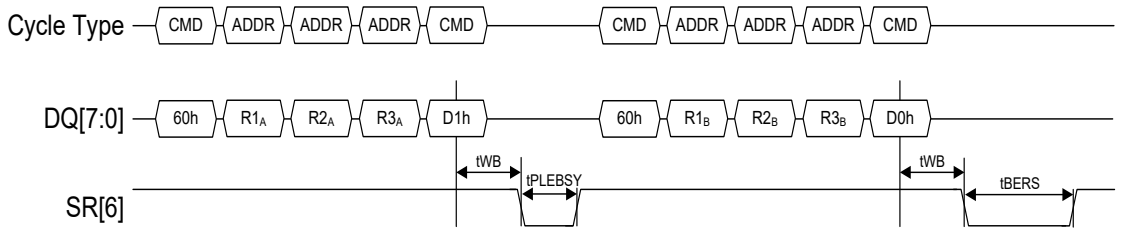


Figure 9-8 Multi-plane Block Erase Timing

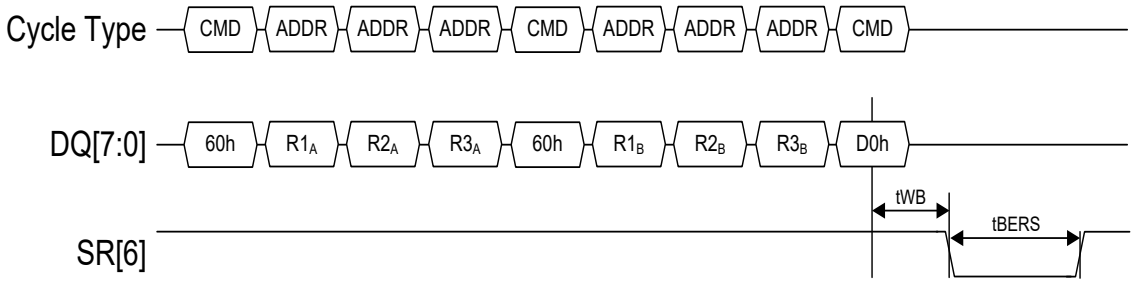


Figure 9-9 Multi-plane Block Erase Timing, ONFI-JEDEC Joint Taskgroup Primary Definition

$R1_A$-$R3_A$ Row address for erase block A. $R1_A$ is the least significant byte.

$R1_B$-$R3_B$ Row address for erase block B. $R1_B$ is the least significant byte.

9.6. Multi-plane Read

The Read command reads a page of data identified by a row address for the LUN specified. The page of data is made available to be read from the page register starting at the column address specified. With a multi-plane operation, multiple reads can be issued back-to-back to the LUN, with a shorter busy time between issuance of the next read operation.

Cache operations may be used when doing multi-plane read operations, as shown, if supported by the target as indicated in the parameter page. Refer to section 6.7.1.27.

Change Read Column Enhanced shall be issued prior to reading data from a LUN. If data is read without issuing a Change Read Column Enhanced, the output received is undefined.

NAND vendors may remove tPLEBSY, tPLPBSY and tPLRBSY busy times, keeping SR[6] HIGH between multi-plane sequences, and instead require the host to provide a vendor specific fixed delay between multi-plane sequences (see vendor datasheet).

The figure below defines the behavior and timings for issuing two multi-plane read commands:

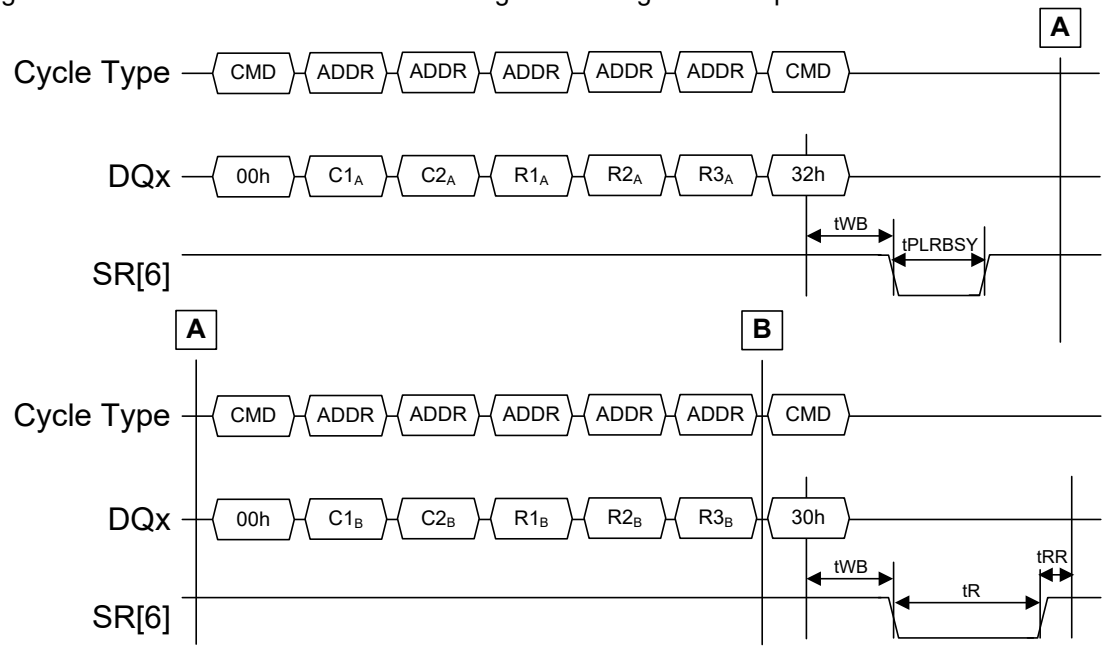


Figure 9-10 Multi-plane Read Timing

$C1_A$-$C2_A$ Column address for page A. $C1_A$ is the least significant byte.

$R1_A$-$R3_A$ Row address for page A. $R1_A$ is the least significant byte.

$C1_B$-$C2_B$ Column address for page B. $C1_B$ is the least significant byte.

$R1_B$-$R3_B$ Row address for page B. $R1_B$ is the least significant byte.

The row addresses for page A and B shall differ in the plane address bits.

The figure below defines the behavior and timings for reading data after the multi-plane read commands are ready to return data:

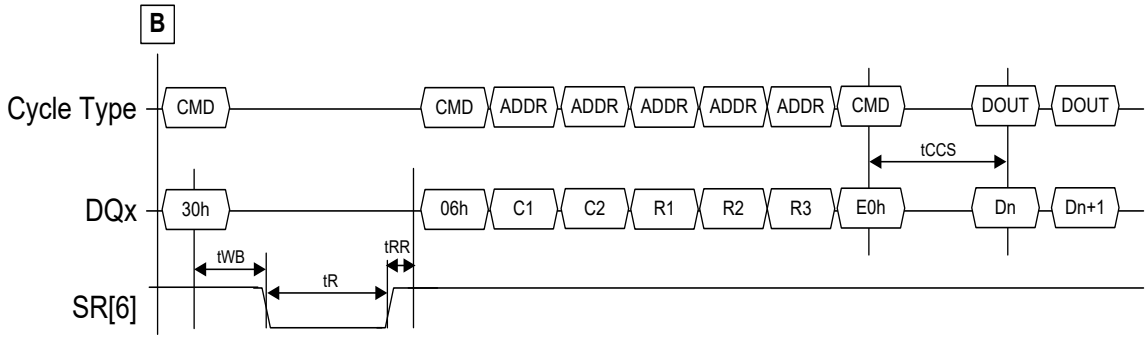


Figure 9-11 Multi-plane Read Data Output With Change Read Column Enhanced Timing

C1-C2	Column address to read from. C1 is the least significant byte.
R1-R3	Row address to read from (specifies LUN and plane address). R1 is the least significant byte.
Dn	Data bytes read starting with addressed row and column.

The row address provided shall specify a LUN and plane address that has valid read data.

For Multi-plane Read Cache Sequential operations, the initial Multi-plane Read command issue is followed by a Read Cache confirmation opcode 31h, as shown in the figure below:

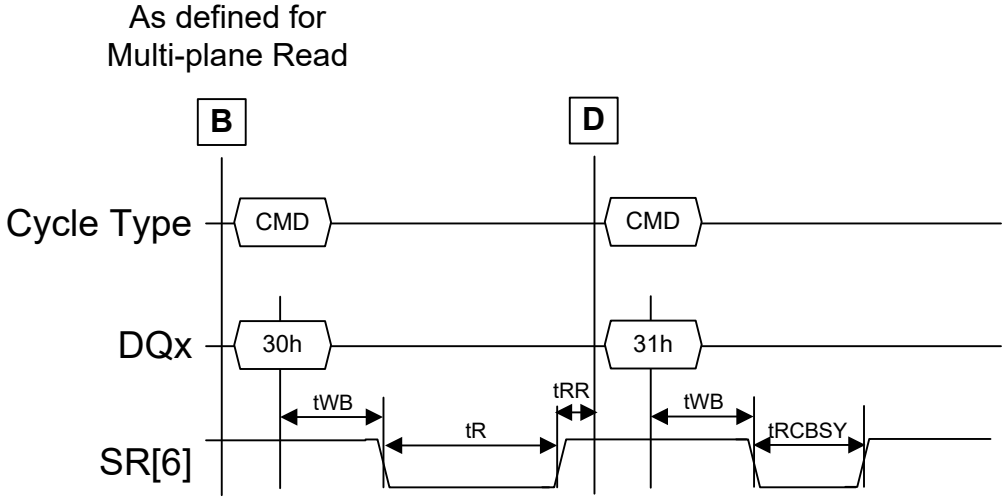


Figure 9-12 Multi-plane Read Cache Sequential Timing

For Multi-plane Read Cache Random operations, the initial multi-plane Read command issue is followed by another Read Multi-plane command sequence where the last confirmation opcode is 31h, as shown in the following figure:

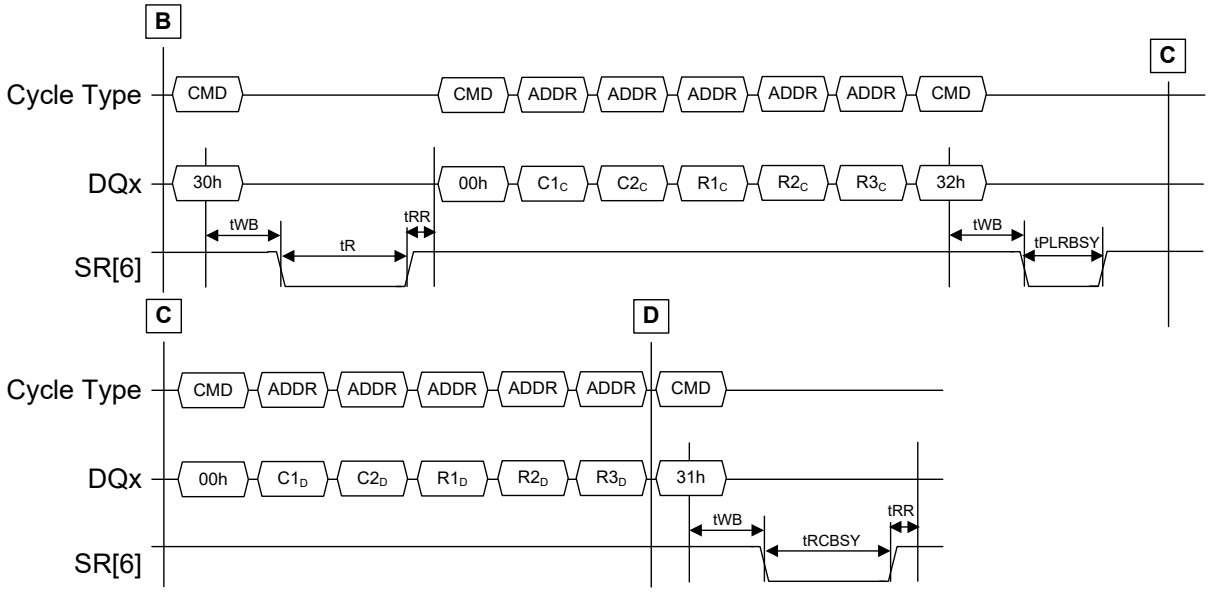


Figure 9-13 Multi-plane Read Cache Random Timing

$C1_C$-$C2_C$ Column address for page C. $C1_C$ is the least significant byte.

$R1_C$-$R3_C$ Row address for page C. $R1_C$ is the least significant byte.

$C1_D$-$C2_D$ Column address for page D. $C1_D$ is the least significant byte.

$R1_D$-$R3_D$ Row address for page D. $R1_D$ is the least significant byte.

The row addresses for page C and D shall differ in the plane address bits.

For Multi-plane Read Cache operations, two data output operations follow each Multi-plane Read Cache operation. The individual data output sequences are described in Figure 9-11. Prior to the last set (i.e. two) data output operations, a Read Cache End command (3Fh) should be issued by the host.

10. APPENDIX: Sample Code for CRC-16 (Informative)

This section provides an informative implementation of the CRC-16 polynomial. The example is intended as an aid in verifying an implementation of the algorithm.

```
int main(int argc, char* argv[])
{
      // Bit by bit algorithm without augmented zero bytes
  const unsigned long crcinit = 0x4F4E; // Initial CRC value in the shift register
  const int order = 16;          // Order of the CRC-16
  const unsigned long polynom = 0x8005; // Polynomial
  unsigned long i, j, c, bit;
  unsigned long crc = crcinit;        // Initialize the shift register with 0x4F4E
  unsigned long data_in;
  int dataByteCount = 0;
  unsigned long crcmask, crchighbit;
  crcmask = ((((unsigned long)1<<(order-1))-1)<<1)|1;
  crchighbit = (unsigned long)1<<(order-1);

  // Input byte stream, one byte at a time, bits processed from MSB to LSB
  printf("Input byte value in hex(eg. 0x30):");
  printf("\n");
  while(scanf("%x", &data_in) == 1)
{    c = (unsigned long)data_in;
     dataByteCount++;
    for (j=0x80; j; j>>=1)
    {bit = crc & crchighbit; crc<<= 1; if (c & j) bit^= crchighbit;       if (bit) crc^= polynom;    }
    crc&= crcmask;   printf("CRC-16 value: 0x%x\n", crc);   } printf("Final CRC-16 value: 0x%x, total data
  bytes: %d\n", crc, dataByteCount); return 0;}
```

11. APPENDIX: ICC/ICCQ Measurement Methodology

11.1. Conv. Protocol ICC Measurement Methodology

This section defines the technique used to measure the ICC parameters defined in section 2.10 for the Conv. Protocol.

The common testing conditions that shall be used to measure the DC and Operating Conditions are defined in the table below:

Parameter	Testing Condition
General conditions	1. Vcc = Vcc(min) to Vcc(max) 2. VccQ = VccQ(min) to VccQ(max) 3. CE_n = 0 V 4. WP_n = VccQ 5. IOUT = 0 mA 6. Measured across operating temperature range 7. N data input or data output cycles, where N is the number of bytes or words in the page 8. No multi-plane operations. 9. Sample a sufficient number of times to remove measurement variability. 10. Sample an equal ratio of page types that exist in a block. A page type is a group of page addresses and is commonly referred to as upper or lower page (or middle page for 3 bits per cell devices). 11. Choose the first good even/odd block pair beginning at blocks 2-3
Array preconditioning for ICC1, ICC2, and ICC3	The array is preconditioned with vendor required random data pattern.
Fixed wait time (no R/B_n polling)	ICC1: tR = tR(max) ICC2: tPROG = tPROG(max) ICC3: tBERS = tBERS(max)

Table 11-1 Conv. Protocol Common Testing Conditions for ICC

The testing conditions that shall be used to measure the DC and Operating Conditions are defined in the table below:

Parameter	NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT)
AC Timing Parameters	tWC = tWC(min) tRC = tRC(avg) tDSC = tDSC(avg) tADL = ~tADL(min) tCCS = ~tCCS(min)
Bus idle data pattern	DQ[7:0] = FFh
Repeated data pattern (Used for ICC4R, ICCQ4R, ICCQ4W and ICC4W)	DQ[7:0] = A5h, AAh, 5Ah, 55h
NOTES: 1. The value of tCK(avg), tRC(avg), and tDSC(avg) used should be the minimum value of the timing modes supported for the device. 2. ICCQ4R testing is performed with default drive strength setting.	

Table 11-2 Conv. Protocol Data Interface Specific Testing Conditions for ICC

The following figures detail the testing procedure for ICC1, ICC2, ICC3, ICC4R, ICC4W, and ICC5:

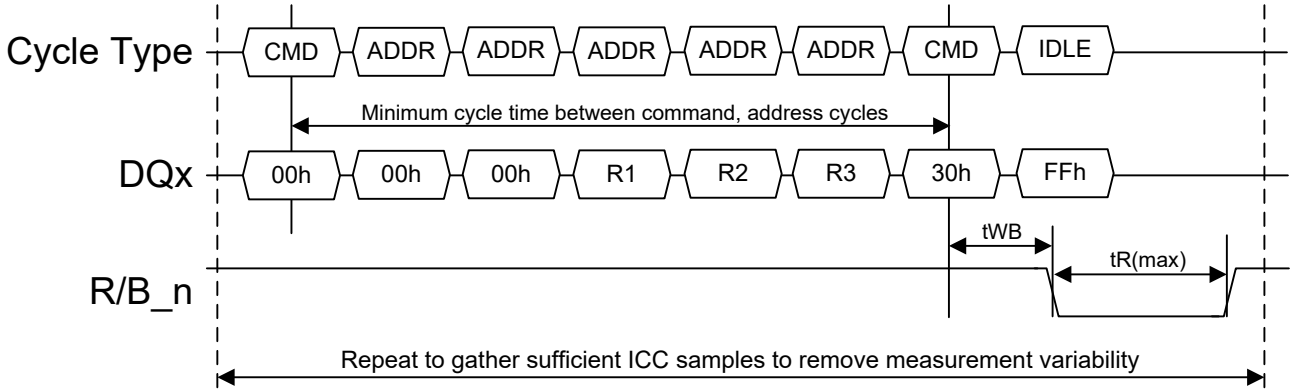


Figure 11-1 Conv. Protocol ICC1 Measurement Procedure

To calculate the active current for ICC1, the following equations may be used.

$$Icc1(measured) = \frac{tR(typ)}{tR(\max)} Icc1(active) + \frac{tR(max) - tR(typ)}{tR(max)} Icc5$$

$$Icc1(active) = \frac{Icc1(measured) \times tR(max)}{tR(typ)} - \frac{Icc5 \times tR(max)}{tR(typ)} + Icc5$$

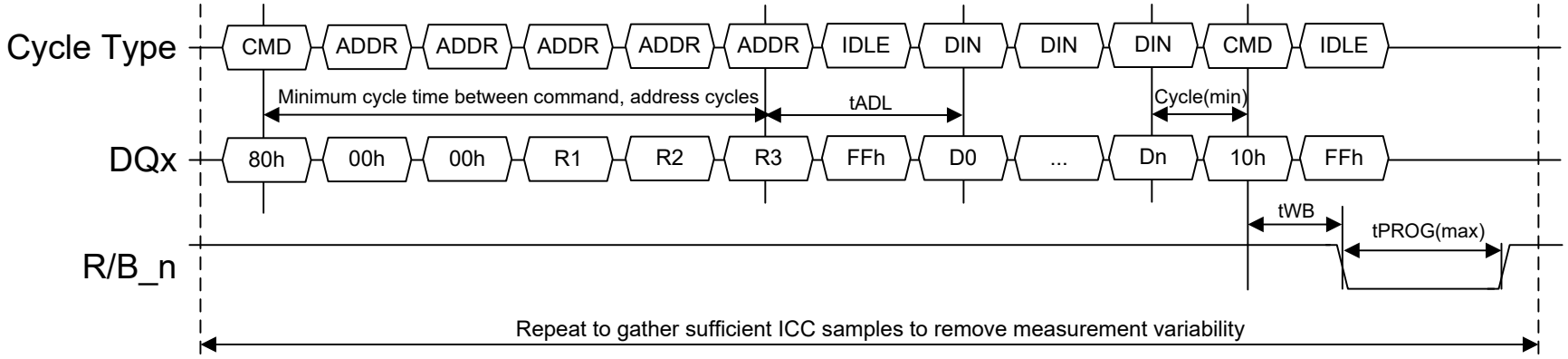


Figure 11-2 Conv. Protocol ICC2 Measurement Procedure

To calculate the active current for ICC2, the following equations may be used.

$$Icc2(measured) = \frac{tIO}{tIO + tPROG(max)} Icc4w + \frac{tPROG(typ)}{tIO + tPROG(max)} Icc2(active) + \frac{tPROG(max) - tPROG(typ)}{tIO + tPROG(max)} Icc5$$

$$Icc2(active) = \frac{Icc2(measured) \times (tIO + tPROG(max)]}{tPROG(typ)} - \frac{tIO \times Icc4w}{tPROG(typ)} - \frac{Icc5 \times tPROG(max)}{tPROG(typ)} + Icc5$$

For the NV-LPDDR4 (LTT) and NV-LPDDR4 with VccQL (PI-LTT) data interfaces, the tIO value is calculated as:

tIO= NAND Page Size(bytes) x (1/2 tDSC(avg))

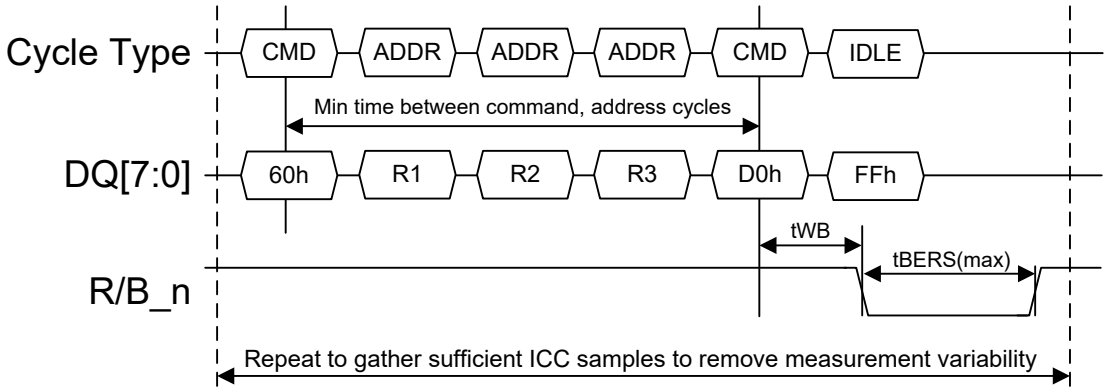


Figure 11-3 Conv. Protocol ICC3 Measurement Procedure

To calculate the active current for ICC3, the following equations may be used.

$$Icc3(measured) = \frac{tBERS(typ)}{tBERS(max)} Icc3(active) + \frac{tBERS(max) - tBERS(typ)}{tBERS(max)} Icc5$$

$$Icc3(active) = \frac{Icc3(measured) \times tBERS(max)}{tBERS(typ)} - \frac{Icc5 \times tBERS(max)}{tBERS(typ)} + Icc5$$

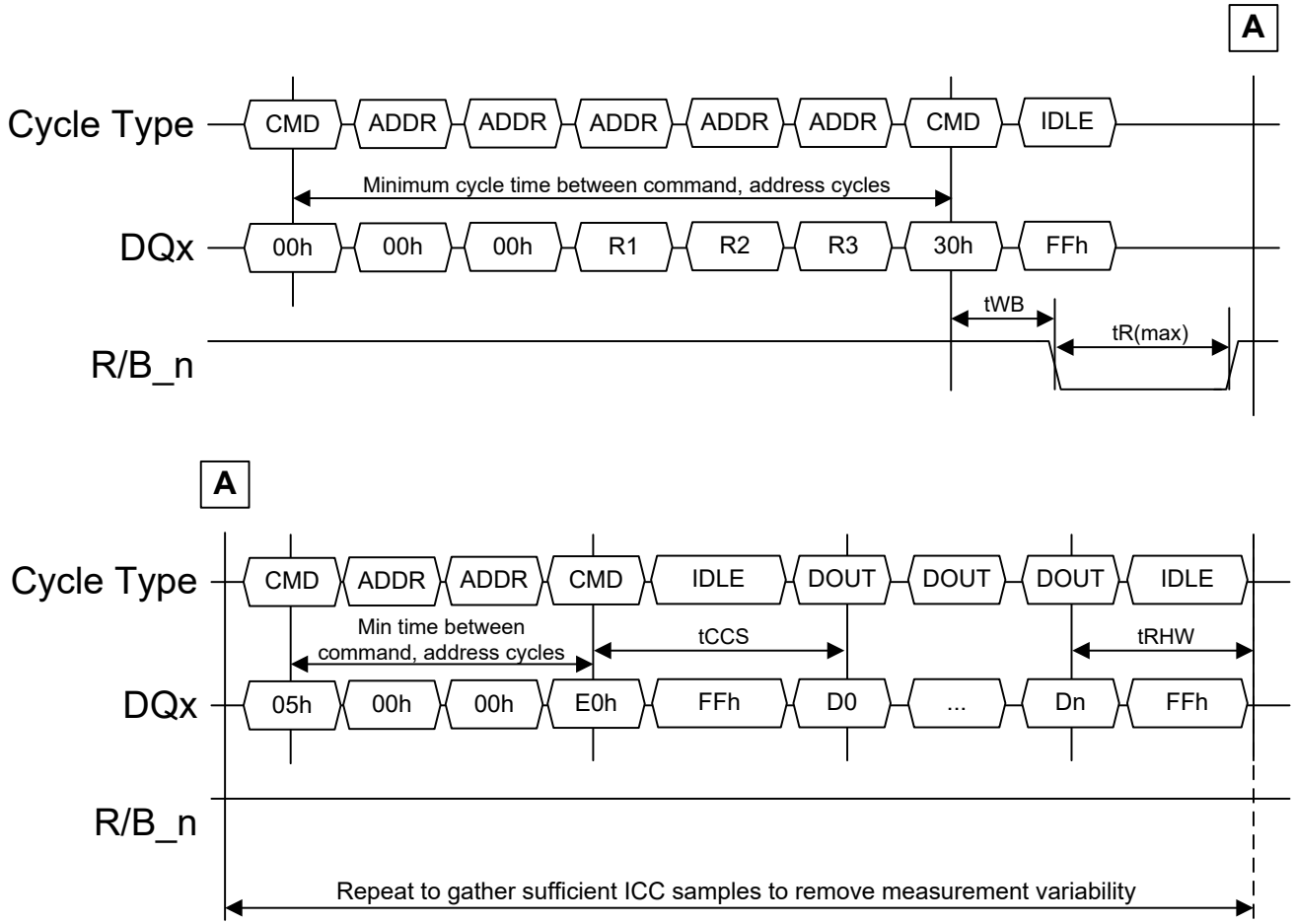


Figure 11-4 Conv. Protocol ICC4R and ICCQ4R Measurement Procedure

NOTE: If the NAND vendor requires the use of Change Read Column Enhanced command for outputting data from the NAND page register, then Change Read Column Enhanced command shall be used for ICC4R and ICCQ4R measurements.

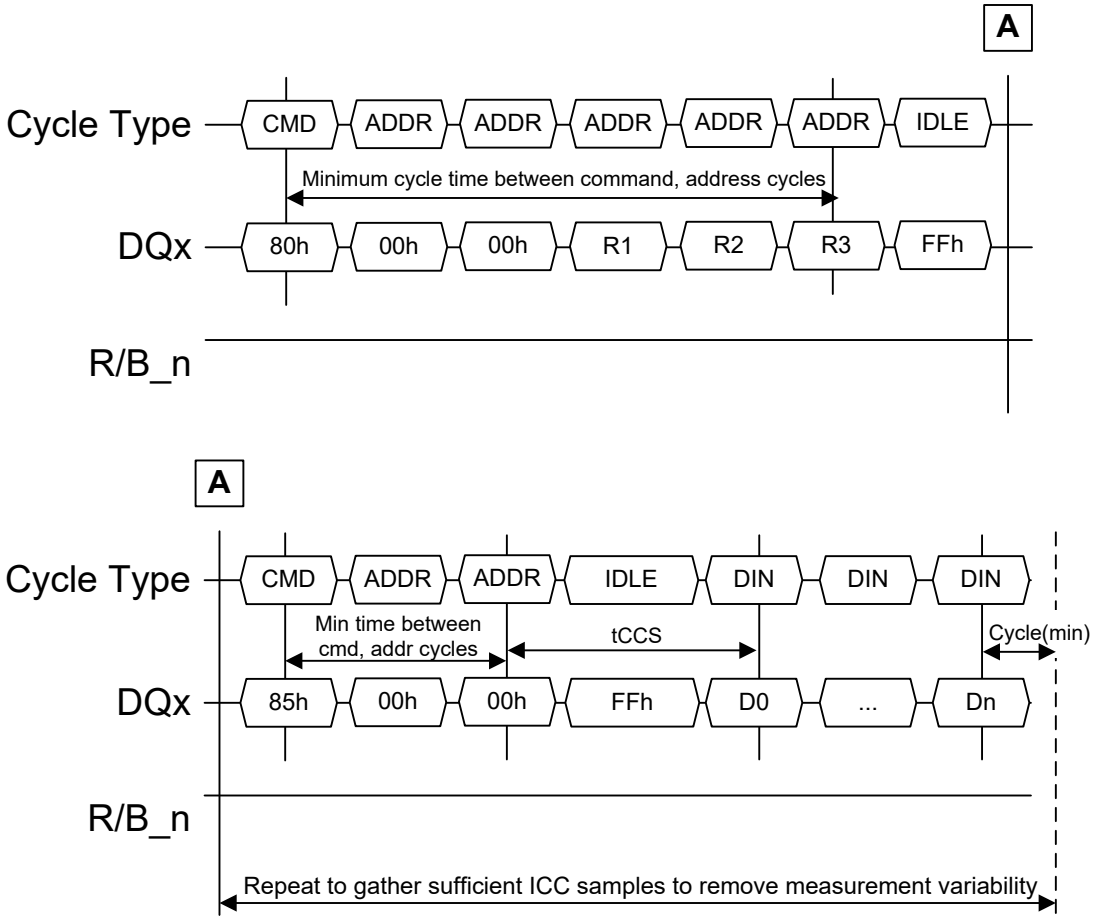


Figure 11-5 Conv. Protocol ICC4W and ICCQ4W Measurement Procedure

NOTE: NAND Vendors may require the host to issue an 11h command to end the 80h sequence first, wait either tPLPBSY time or a vendor specific fixed delay prior to issuing the Change Write Column or Change Row Address command (see vendor datasheet).

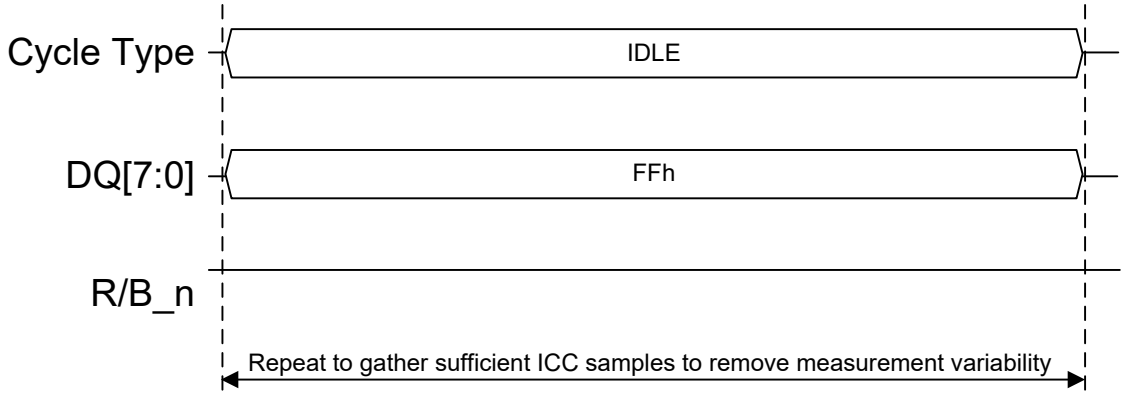


Figure 11-6 Conv. Protocol ICC5 Measurement Procedure

11.2. SCA Protocol Icc/IccQ Measurement Methodology

This section defines the technique used to measure the ICC parameters defined in section 2.10 for the SCA Protocol.

The common testing conditions that shall be used to measure the DC and Operating Conditions are defined in the table below:

Parameter	Testing Condition
General conditions	1. SCA protocol is enabled 2. Vcc = Vcc(min) to Vcc(max) 3. VccQ = VccQ(min) to VccQ(max) 4. WP_n = VccQ 5. IOUT = 0 mA 6. Measured across operating temperature range 7. N data input or data output cycles, where N is the number of bytes or words in the page 8. No multi-plane operations. 9. Sample a sufficient number of times to remove measurement variability. 10. Sample an equal ratio of page types that exist in a block. A page type is a group of page addresses and is commonly referred to as upper or lower page (or middle page for 3 bits per cell devices). 11. Choose the first good even/odd block pair beginning at blocks 2-3 12. DBI is disabled
Array preconditioning for Icc1, Icc2, and Icc3, IccQ1, IccQ2, IccQ3, Isb and IsbQ	The array is preconditioned with vendor required random data pattern.

Table 11-3 SCA Protocol Common Testing Conditions for ICC

The testing conditions that shall be used to measure the DC and Operating Conditions are defined in the table below:

Parameter	NV-LPDDR4 (LTT) / NV-LPDDR4 with VccQL (PI-LTT)
AC Timing Parameters	tCACI = tCACI(min) tCDL = tCDL(min) tCCS = tCCS(min) tDSC = tDSC(avg) tLUNSEL_CA = tLUNSEL_CA (min) tRC = tRC(avg)
Repeated data pattern (Used for Icc4R, IccQ4R, Icc4W and IccQ4W)	DQ[7:0] = Randomized data pattern as required by NAND vendor array
NOTES: 1. The value of tRC(avg), and tDSC(avg) used should be the minimum value of the timing modes supported for the device. 2. IccQ4R testing is performed with default drive strength setting.	

Table 11-4 SCA Protocol Data Interface Specific Testing Conditions for ICC

The following figures detail the testing procedure for Icc1, Icc2, Icc3, Icc4R, Icc4W, Icc5, Isb, IccQ1, IccQ2, IccQ3, IccQ4R, IccQ4W, IccQ5, IsbQ:

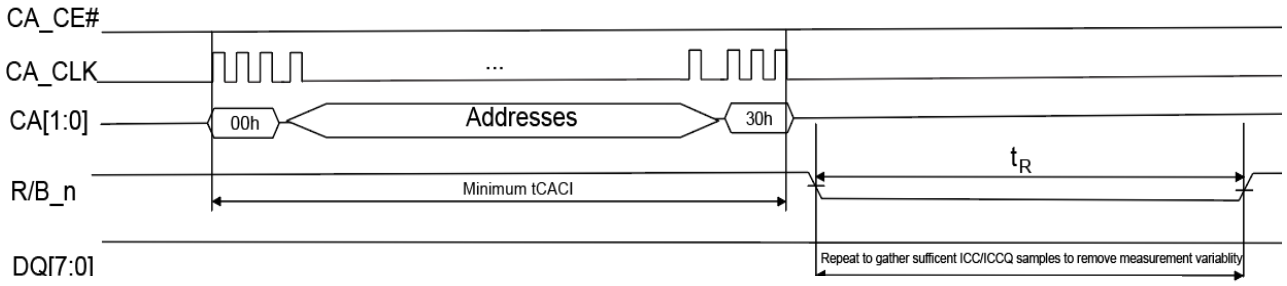


Figure 11-7 SCA Protocol Icc1 and IccQ1 Measurement Procedure

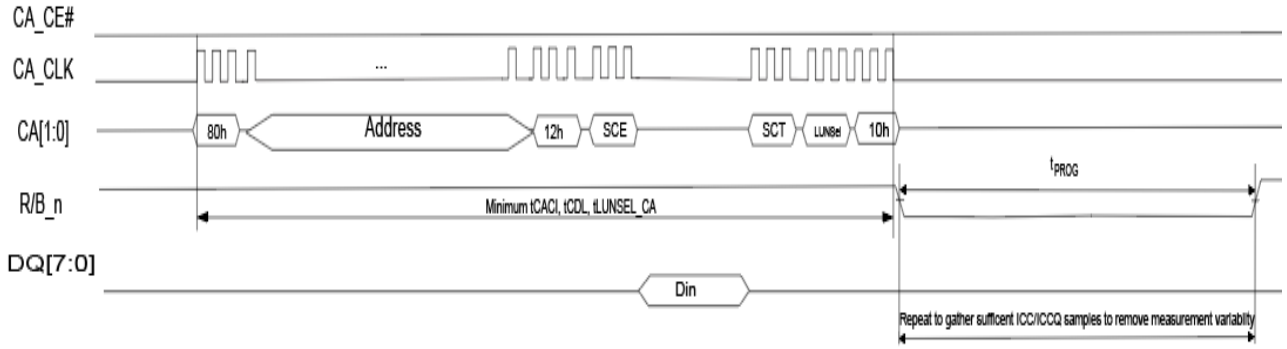


Figure 11-8 SCA Protocol Icc2 and IccQ2 Measurement Procedure

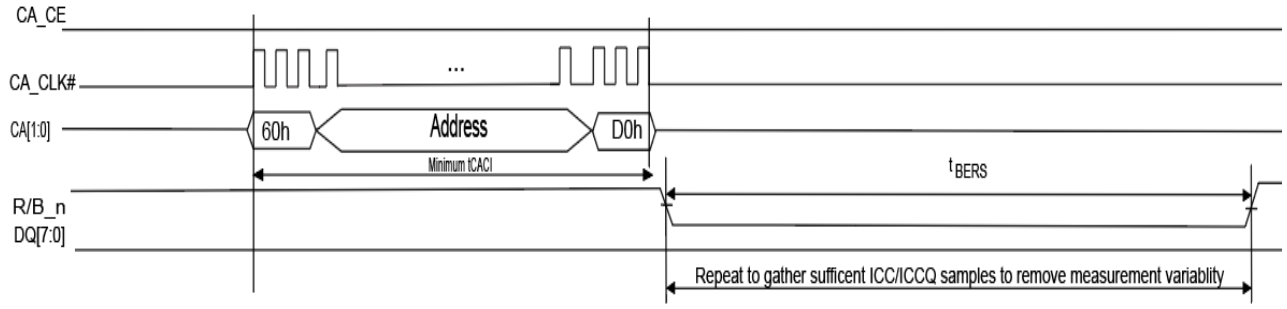


Figure 11-9 SCA Protocol Icc3 and IccQ3 Measurement Procedure

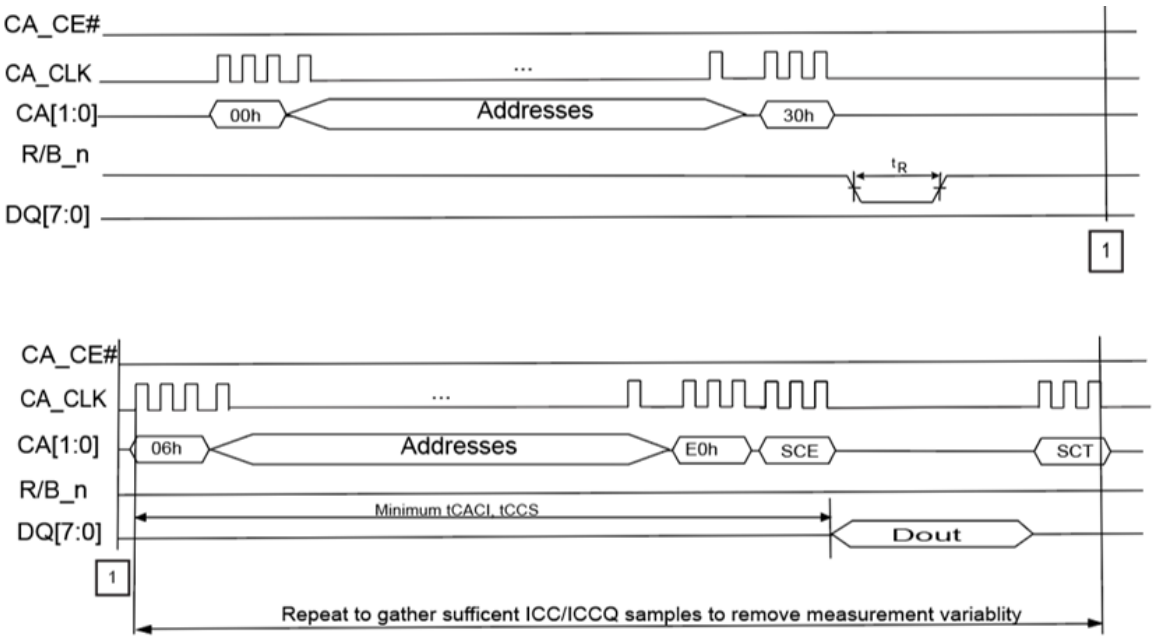


Figure 11-10 SCA Protocol Icc4R and IccQ4R Measurement Procedure

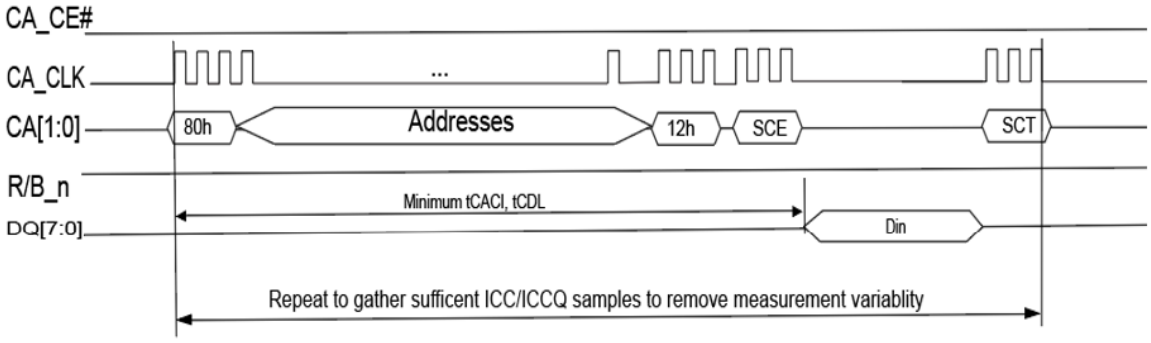


Figure 11-11 SCA Protocol Icc4W and IccQ4W Measurement Procedure

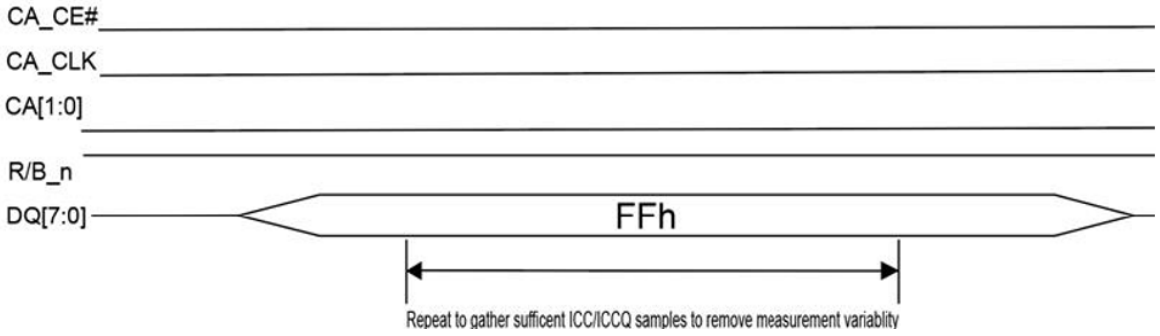


Figure 11-12 SCA Protocol Icc5 and IccQ5 Measurement Procedure

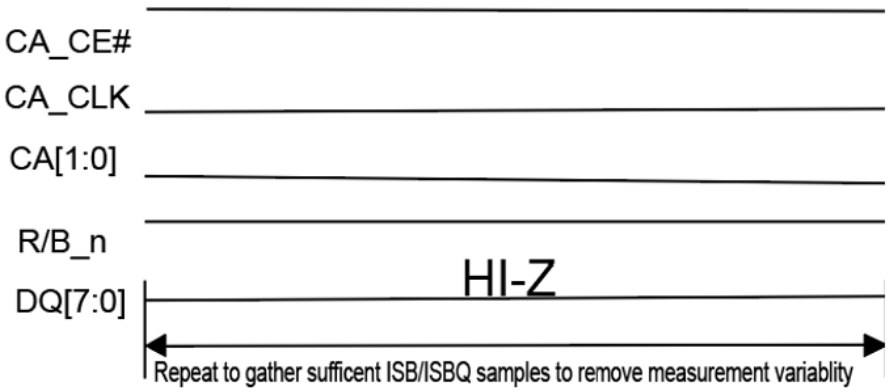


Figure 11-13 SCA Protocol Isb and IsbQ Measurement Procedure

12. APPENDIX: Measuring Timing Parameters to/from Tri-State

There are several timing parameters that are measured to or from when:

- The device is no longer driving the NAND bus or a tri-state (hi-Z) condition
- The device begins driving from a tri-state (hi-Z) condition

Examples of such timing parameters are: tDQSD, tDQSHZ, tCHZ.

This appendix defines a two-point method for measuring timing parameters that involve a tri-state condition. The figure below defines a method to calculate the point when the device is no longer driving the NAND bus or begins driving by measuring the signal at two different voltages. The voltage measurement points are acceptable across a wide range (*x* = 20 mV up to *x* < 1/4 of VccQ). The figure uses tDQSHZ and tDQSD as examples. However, the method should be used for any timing parameter that specifies that the device output is no longer driving the NAND bus or specifies that the device begins driving the NAND bus from a tri-state condition.

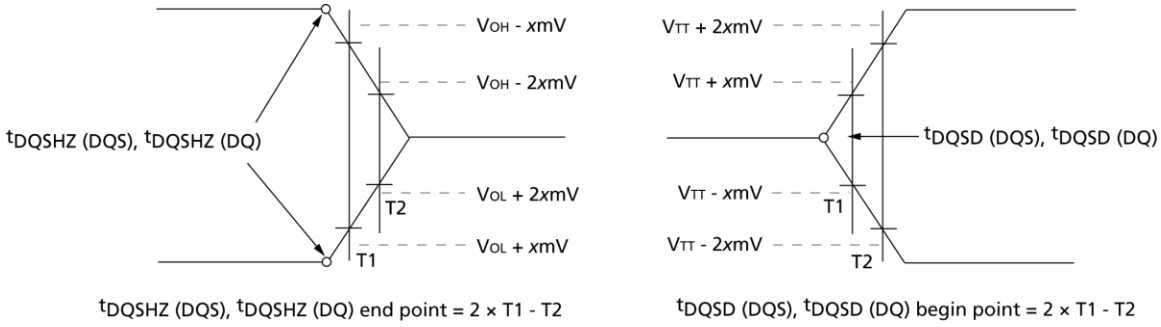


Figure 12-1 Two-point Method for Measuring Timing Parameters with Tri-state Condition